

Problem 1: (20 points)

- (a) (4%) Show that the set {AND, OR, NOT} of logic operations is *functionally complete*, that is, any Boolean function can be represented with this set of logic operations.
- (b) (4%) Is the set consisting of only majority gate MAJ *functionally complete*? Justify your answer.
 (Note that the majority gate MAJ(a, b, c) with three inputs a, b, c equals 1 if and only if at least two of the inputs are 1.)
- (c) (4%) Is the set consisting of only minority gate MIN *functionally complete*? Justify your answer.
 (Note that the minority gate MIN(a, b, c) with three inputs a, b, c equals 1 if and only if at most one of the inputs is 1.)
- (d) (4%) Can any Boolean function be represented in the *exclusive-sum-of-products* (ESOP) expression, which is the AND-XOR two-level expression (with first level AND and second level XOR)? Justify your answer.
- (e) (4%) Can any Boolean function be represented in the *exclusive-product-of-sums* (EPOS) expression, which is the XOR-AND two-level expression (with first level XOR and second level AND)? Justify your answer.

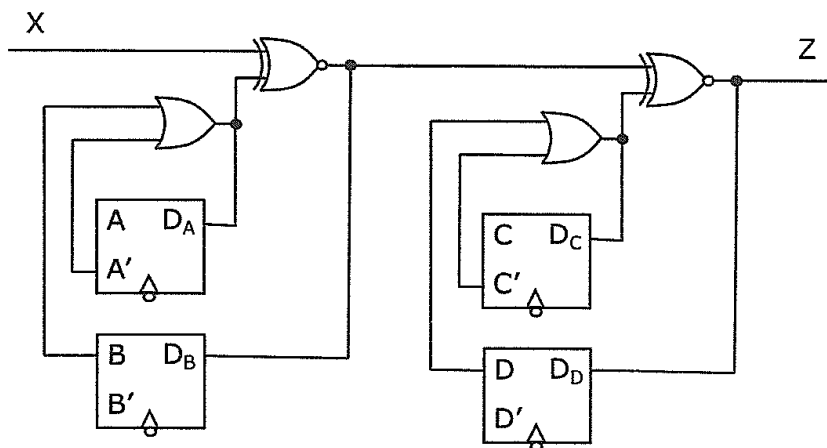
Problem 2: (20 points)

Consider the expression $X_1 \oplus X_2 \oplus \dots \oplus X_n$.

- (a) (10%) Prove by induction that it represents an odd-parity function, that is, it evaluates to 1 if and only if the assignment to variables X_1, \dots, X_n contains an odd number of 1's. (For example, the assignment $(X_1, X_2, X_3, X_4) = (1, 0, 0, 0)$ contains one 1.)
- (b) (5%) How many product terms are there for its minimum sum-of-products (SOP) expression?
- (c) (5%) How many sum terms are there for its minimum product-of-sums (POS) expression?

Problem 3: (20 points)

Consider the following sequential circuit.



Assume that the four D-flip-flops are triggered by the same clock signal, the flip-flop propagation delay is 1 ns, the flip-flop setup time is 2 ns, the input signal X has delay 2 ns, the OR gate has delay 3 ns, and the XOR gate has delay 4 ns.

- (a) (5%) Determine the minimum clock cycle that the circuit can operate.
- (b) (5%) Determine the constraint on the flip-flop hold time for the circuit to operate correctly.
- (c) (5%) Assume the combinational part of the circuit is to be re-implemented by a single read-only memory (ROM). Determine the size of the ROM in terms of 1) the number of words and 2) the bit-width of each word.
- (d) (5%) Assume the circuit is initially in state $(A, B, C, D) = (0, 0, 0, 0)$. Determine the corresponding state-transition sequence and output sequence with respect to the input sequence 0, 1, 1.

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Problem 4: (20 points)

Design a Moore sequential circuit with input X and output Z that meets the following requirement.

Z = 1, if there are at least two 1's appearing in the last three inputs, and

Z = 0, otherwise.

Example

X = 001101100101000...

Z = 000111110001000...

- (a) (10%) Draw the corresponding state graph and identify all equivalent states, if there is any, for state minimization.
- (b) (10%) Implement the circuit with three D flip-flops and one majority gate MAJ.

Problem 5: (20 points)

Given two Mealy sequential circuits, let M_1 have four states A, B, C, D and M_2 have four states S, T, U, V. Assume the implication table (or pair chart) for the state pairs between M_1 and M_2 is as follows (where an entry with a cross sign indicates the output difference for the corresponding state pair between M_1 and M_2 , and the expression "Y-Z" in a (W,X)-entry indicates that the next-state pair (Y, Z) must be equivalent in order for the corresponding current-state pair (W,X) to be equivalent).

	S	T	U	V
A	B-S C-U	X	B-U C-V	X
B	A-S C-U	X	A-U C-V	X
C	X	C-T D-T	X	C-V D-S
D	D-S B-U	X	D-U B-V	X

- (a) (5%) Find all possible initial state pairs between M_1 and M_2 that make the two circuits behave the same.
- (b) (5%) Let M_1 starts from state C and M_2 starts from state T. What is the minimum length of an input sequence that makes M_1 and M_2 produce different outputs? Justify your answer.
- (c) (5%) Are there equivalent states in M_1 ? If yes, which states are equivalent?
- (d) (5%) Assume S is the initial state of M_2 . Identify all the states in M_2 that can be reached from S. (We say that state A can reach state B if there exists a sequence of state transitions from A to B.)

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