題號： 391　　　國立臺灣大學 110 學年度碩士班招生考試試題
科目：控制系統(C)
節次： 7

1. Figure 1 shows a non-ideal operational amplifier with negative feedback. Show the configuration of this circuit connection is unstable. (15%)

2. In Fig. 2, the request task is to design a unity feedback controller for a 1st order plant. The requirement is to design the controller so that the closed-loop poles lie within the shaded regions.
   (a) What values of ω_n and ξ correspond to the shaded regions? (6%)
   (b) Let $K_a = \text{a} = 2$. Find values for K and K_I so that the poles of the closed-loop system lie within the shaded regions. (6%)
   (c) Demonstrate that no matter what the value of K_A and A are, the controller provides enough flexibility to place the poles anywhere in the left-half plane. (8%)

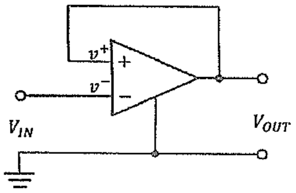

Fig. 1.

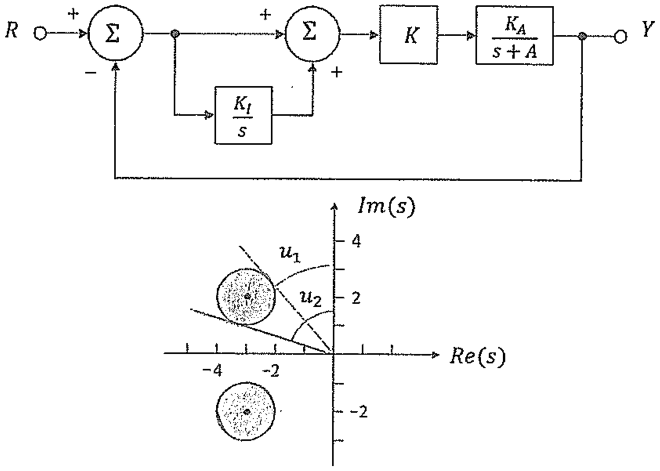

Fig. 2.

3. Modify the Routh criteria so that it can apply to the case in which all the poles are to be to the left of α when α > 0 to the polynomial: $s^3 + (6 + K)s^2 + (5 + 6K) + 5K = 0$, with the assume value of α= 1. (15%)

4. Consider the state equation: $\dot{x} = \begin{bmatrix} 0 & 1 \\ 7 & -4 \end{bmatrix} x + \begin{bmatrix} 1 \\ 2 \end{bmatrix} u$,　$y = [1 \quad 3]x$
   (a) Draw the block diagram for the plant with the condition that one integrator for each state variable. (4%)
   (b) Find the transfer function. (4%)
   (c) Find the closed-loop characteristic equation if the "state feedback" is $u = -[K_1 \quad K_2]x$; (6%)
   (d) Find the closed-loop characteristic equation if the "output feedback" is $u = -\text{K} \cdot \text{y}$. (6%)

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5. Consider the electric circuit shown in Fig. 3.
   (a) Write the state equation for the circuit. The input u(t) is current, and the output y is voltage. Let $x_1 = i_L$ and $x_2 = v_c$. (5%)
   (b) What condition on R, L, and C will guarantee that the system is "controllable"? (5%)
   (c) What condition on R, L, and C will guarantee that the system is "observerable"? (5%)

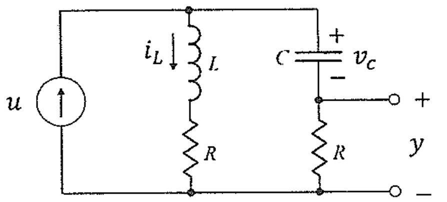

Fig. 3.

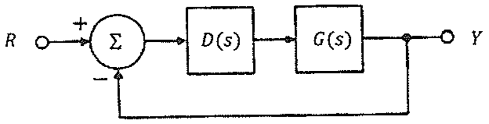

Fig. 4.

6. Assume the closed-loop system of Fig. 4 has a feedforward transfer function given by $G(s) = \frac{1}{s(s+2)}$. Design a lag compensator *D(s)* so that the dominant poles of the closed-loop system are located at $s = -1 \pm j$ and the steady-state error to a unit ramp input is less than 0.2. (15%)

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