

單選題 (每題 5 分)

請用 2B 鉛筆作答於答案卡，並先詳閱答案卡上之「畫記說明」。

1. A processor has a direct mapped cache. Each cache block holds 8 words of data. Data words are 4-byte long. Data addresses are to the byte. A physical address is 32 bits long. The tag is 21 bits. How many blocks are in this cache?  
(A) 8 (B) 16 (C) 32 (D) 64 (E) 128
2. A processor has a four-way set associative L1 data cache of 8 KByte in size, with 64-byte cache blocks. The physical address is 32 bits and data addresses are to the byte. How many bits will be for the tag field?  
(A) 18 (B) 19 (C) 20 (D) 21 (E) 22
3. Consider a two-level cache for a processor. L1 cache and L2 cache have relative hit rates of 95% and 82% respectively. Access times of L1, L2, RAM are 1 ns, 10 ns, and 100 ns. What is the average access time in ns?  
(A) 2.01 (B) 2.26 (C) 3.7 (D) 22.15 (E) 27.15
4. What statement is false about Virtual File System (VFS) in Linux kernel?  
(A) VFS provides the filesystem interface to kernel space programs.  
(B) VFS provides an abstraction within the kernel to allow different filesystem implementations to coexist.  
(C) VFS serves as the filesystem interface to user space programs.  
(D) VFS need some directory entry cache in memory for performance.

For problems 5~8, consider a multi-level memory management scheme using paging with 32-bit page table entries, 46-bit virtual addresses, and a page size of 8 KByte.

5. How many pages are in the virtual address space?  
(A)  $2^{30}$  (B)  $2^{31}$  (C)  $2^{32}$  (D)  $2^{33}$  (E)  $2^{34}$
6. If each individual page table, at each level, must fit in a single page frame, how many levels will be required at least in the scheme.  
(A) 1 (B) 2 (C) 3 (D) 4 (E) 5
7. Suppose that each individual page table, at each level, must fit in a single page frame and that a particular process uses only 2 GBytes of virtual memory. How many individual page tables, at bottom most level, will be required to translate this process' address space?  
(A)  $2^6$  (B)  $2^7$  (C)  $2^8$  (D)  $2^{18}$  (E)  $2^{22}$
8. If the physical memory space is 32 GBytes. What will be the minimum size in bits of each entry of a fully-associative TLB (Translation Lookahead Buffer) for this management scheme?  
(A) 16 (B) 32 (C) 48 (D) 64 (E) 128
9. To make better use of the computer's resources, an operating system can give  
(A) higher (B) lower (C) the same (D) random  
priority to I/O-bound programs than or between the CPU-bound programs.
10. We can use semaphores to deal with the critical-section problem. There are  $n$  processes sharing a semaphore object whose value need to be initialized to  
(A)  $n$  (B) 1 (C) 0 (D) -1 (E) 2
11. A UNIX filesystem has 2 KByte blocks and 4-byte disk addresses. Each inode contains 10 direct entries, one singly indirect entry and one doubly indirect entry. What is the maximum file size in an approximate value?  
(A) 1 GByte (B) 4 GByte (C) 400 MByte (D) 500 MByte (E) 800 MByte
12. Assume that we will use multi-core processor to solve a problem in parallel and 95% of the program code is parallelizable. If we want to get a speedup of 8, how many cores are needed at least?  
(A) 9 (B) 10 (C) 11 (D) 12 (E) 13

見背面

13. Consider a pipelined datapath to process instructions and is consisted of five steps: Fetch instruction, Decode instruction, Execute instruction, Memory access, Write Back and the processing times are 0.4 ns, 0.25 ns, 0.2 ns, 0.4 ns, and 0.33 ns, respectively. If we want to design a control circuit to operate the pipelined datapath, what is the clock rate?  
(A) 2.5 GHz (B) 4 GHz (C) 5 GHz (D) 3 GHz
14. A key difference between symmetric multiprocessors and systems built out of several multicore processors is that  
(A) the communication latency between two cores is not constant  
(B) Cache coherence protocol is required  
(C) Cache replacement policies is required  
(D) Translation lookahead buffer is better used
15. We can implement the wait() and signal() semaphore operations in multiprocessor using  
(A) virtualization instruction  
(B) arithmetic instruction  
(C) test-and-set instruction  
(D) logic instruction  
(E) vector instruction

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16. Which of the following scheduling algorithms could result in starvation?  
(A) First-come, first-served  
(B) Round robin  
(C) Shortest job first  
(D) Priority-based
17. Which scheduling algorithms would discriminate in favor of short processes?  
(A) First-come, first-served  
(B) Round robin  
(C) Multi-level feedback queues  
(D) Priority-based
18. What features are suitable to describe linked disk allocation algorithms.  
(A) Space wasted in index block  
(B) Inefficient for random access  
(C) Suffers external fragmentation  
(D) Suffers internal fragmentation if initial file size allocation is large.  
(E) Unreliable because single error can cause loss of many blocks of data.
19. What are the two main components of the disk access time in disk scheduling?  
(A) Seek time  
(B) DMA control latency  
(C) CPU data bus hold time  
(D) Rotational latency  
(E) Pipeline latency
20. What are three main characteristic of RISC processors?  
(A) Simpler instruction, hence mostly using hardwired decoding.  
(B) Instruction with abundant addressing modes.  
(C) Most instructions take single clock cycle to get executed.  
(D) More number of general purpose registers.  
(E) ALU instructions support both register and memory operands.