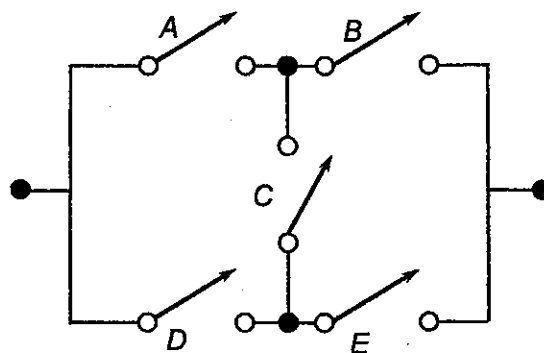


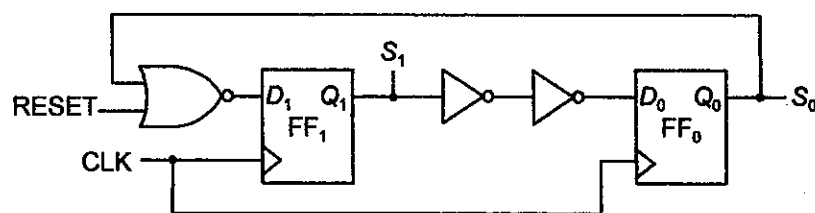
1. (20%) Given a Boolean function $f(a, b, c, d)$ with the properties $f(a, b, c, d) = f(b, a, c, d)$ and $f(a, b, c, d) = f(a, c', b', d)$ (notice the complements), suppose f is partially known as shown in the following Karnaugh map.

cd \ ab	00	01	11	10
00	0			
01			0	1
11		1		
10			0	

- (a) (11%) Which of the unknown minterms ($m_1, m_2, m_3, m_4, m_5, m_6, m_8, m_{10}, m_{11}, m_{12}, m_{15}$) are uniquely determined? What are their values (please indicate all known values in a Karnaugh map)?
- (b) (4%) How many functions satisfy the above constraints?
- (c) (5%) Among these functions, which one has the simplest sum-of-product (SOP) expression?
2. (15%) Consider a Boolean function f such that $f = x_2'x_3 + x_2x_4$ when $x_1 = 0$, $f = x_3x_4'$ when $x_1 = 1$ and $x_2 = 0$, and $f = x_3 + x_4'$ when $x_1 = 1$ and $x_2 = 1$.
- (a) (10%) Draw the Karnaugh map and express f in minimum sum of products (SOP).
- (b) (5%) If the minimum SOP expression obtained in (a) is implemented by a two-level AND-OR circuit, does it suffer from static 1-hazards? If yes, explain why and how to fix the problem. Otherwise, explain why not.
3. (10%) Consider the following switching network consisting of five switches.



- (a) (5%) Give a minimum sum-of-product (SOP) Boolean expression describing the condition that the left and right terminals are connected.
- (b) (5%) Give a minimum product-of-sum (POS) Boolean expression describing the condition that the left and right terminals are connected.
4. (16%) The following circuit diagram implements a finite state machine (FSM) with two state bits, S_0 and S_1 :



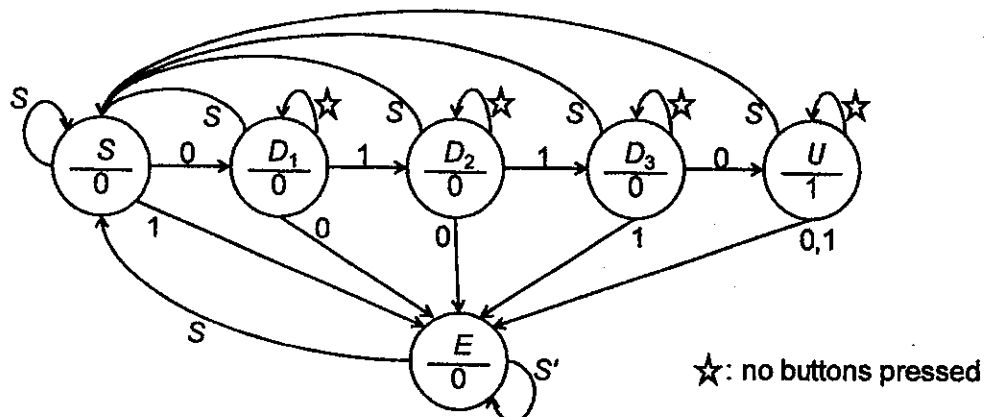
- (a) (4%) Assume the propagation delays (delay from clock edge to Q), setup times, and hold times of rising-edge triggered D flip-flops are 2ns, 3ns, and 1ns, respectively. Assume the delays of inverter and NOR

見背面

gates are $2ns$ and $2ns$, respectively. Assume wire (interconnect) delays are zero. What is the smallest clock period for which the circuit still operates correctly?

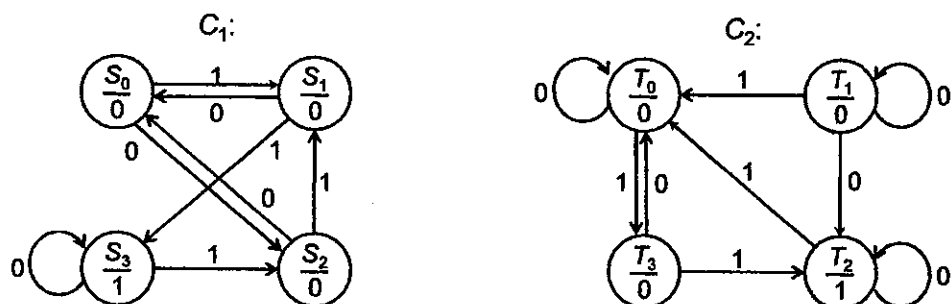
- (b) (4%) A sharp-eyed student suggests optimizing the circuit by removing the pair of inverters and connecting Q_1 directly to D_0 . If the clock period can be adjusted appropriately, would the optimized circuit operate correctly? If yes, explain the adjustment to the clock period that would be needed.
- (c) (4%) When the RESET signal is set to "1" for several cycles, what state is the FSM set to? (Give values of S_0 and S_1 .)
- (d) (4%) Suppose there is skew in the CLK signal such that the rising edge of CLK always arrives at FF_1 exactly $1ns$ before it arrives at FF_0 . What is the smallest clock period for which the FSM still operates correctly?

5. (19%) The following figure shows a digital lock design based on a 6-state finite state machine (FSM). The design has three buttons labeled "0", "1", and "S" (Start), and generates an unlock signal (output) $U=1$ when the user presses S followed by the sequence 0, 1, 1, 0.



- (a) (6%) This design can be further simplified by removing the "S" button. Please design a Moore FSM whose inputs are simply "0" and "1" buttons, whose output is the U (unlock) signal, and which has the property that $U=1$ if and only if the last four button presses correspond to the sequence 0,1,1,0. Show the state transition diagram with fewest states corresponding to your design. (No partial credits for a FSM with more states.)
- (b) (4%) Is it possible that an equivalent FSM might be implemented in fewer than 5 states? Explain.
- (c) (4%) D flip-flops are used to hold your FSM states, and they contain random values when power is first applied to your lock. Does this constrain your handling of unused states? Explain and show your modified FSM state transition diagram.
- (d) (5%) Use a ROM and several D flip-flops to implement your FSM. Completely specify the ROM contents including those corresponding to unused states.

6. (20%) Let C_1 and C_2 be two sequential circuits with states $\{S_0, S_1, S_2, S_3\}$ and $\{T_0, T_1, T_2, T_3\}$, respectively, whose transitions are shown in the figure below.



- (a) (5%) How many non-equivalent states are there in C_1 ? Which states are equivalent in C_1 ?
- (b) (5%) How many non-equivalent states are there in C_2 ? Which states are equivalent in C_2 ?
- (c) (5%) If C_1 and C_2 start from states S_0 and T_0 , respectively, are these two circuits equivalent (in terms of input-output behavior)? If yes, briefly explain why. Otherwise, identify an input sequence that distinguishes C_1 and C_2 .
- (d) (5%) Redo (b) for C_1 and C_2 starting from states S_0 and T_1 , respectively.