複選題，每題皆有一個或多個正確答案，未答視同放棄該題、得0分，既答題每個正確答案可得2分，每個錯誤答案倒扣1分，每題最多倒扣5分。

1. (10%) Which of the following statements are true regarding virtual memory management?
   (a) When a process is not allocated enough frames to contain its working set, performance may drop drastically.
   (b) OS checks the program of each process to calculate its working set for the duration of the process execution.
   (c) Locality of memory reference is crucial to the performance of virtual memory management.
   (d) The copy-on-write strategy can save precious time in process creation.
   (e) None of the above are true.
2. (10%) Which of the following statements regarding serializability are true?
   (a) A serial schedule guarantees that each transaction is executed atomically.
   (b) A non-serial schedule does not necessarily imply an incorrect execution.
   (c) One protocol that ensures serializability is the two-phase locking protocol.
   (d) The timestamp-ordering protocol ensures conflict serializability since conflicting operations are processed in timestamp order.
   (e) None of the above are true.
3. (10%) Which of the following statements about synchronization are true?
   (a) If the wait and signal operations are not executed atomically, then mutual exclusion may be violated.
   (b) If the conditions of mutual exclusion, hold and wait, no preemption, and circular wait hold simultaneously in a system, then a deadline situation must arise.
   (c) Spinlocks are not appropriate for uniprocessor systems.
   (d) Semaphores and conditional critical regions are equivalent.
   (e) None of the above are true.
4. (10%) Which of the following statements are true?
   (a) Cache memory is used in addition to main memory for better storage stability.
   (b) Disks are used in the storage hierarchy for better storage stability.
   (c) Disks are used in the storage hierarchy because they are cheaper per bit.
   (d) The cache coherence problem adds to the complexity of control hardware in storage hierarchy.
   (e) None of the above are true.
5. (10%) Suppose we have a benchmark that executes in 100 seconds of elapsed time, where 90 seconds are CPU time, and the rest is I/O time. If CPU time improves by 50% per year for the next years, but I/O time does not improve, then which of the following statements are true?
   (a) By the end of the 1st year, we will be able to speed up the execution time of this benchmark by a factor of $2\times$.
   (b) By the end of the 2nd year, the percentage of the execution time spent on I/O will double.
   (c) By the end of the 3rd year, we will be able to speed up the execution time of this benchmark by a factor of $3\times$.
   (d) By the end of the 5th year, more than 50% of the execution time of this benchmark will be spent on I/O.
   (e) None of the above are true.
6. (10%) Which of the following statements are true?
   (a) After a user program starts an I/O operation, it must always wait for the completion of the I/O operation to resume its program execution.
   (b) On a typical computer system, interrupt vector tells us the port addresses of an I/O controller.
   (c) DMA needs to work with device polling mechanism in order to achieve maximal efficiency.
   (d) Data movement between I/O devices and the main memory usually are executed in CPU to enhance I/O performance.
   (e) None of the above are true.

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7. (10%) Which of the following instructions are usually implemented as privileged instructions?
   (a) Test-and-set instructions.
   (b) I/O instructions.
   (c) Floating-point instructions.
   (d) MMU manipulation instructions.
   (e) None of the above.

8. (10%) Which of the following properties are the advantages of user threads over kernel threads?
   (a) Efficiency in context switch.
   (b) Efficiency in thread creation.
   (c) Efficiency in message passing.
   (d) Responsiveness: allowing a program to continue to run even if some of its threads are blocked.
   (e) None of the above.

9. (10%) A pipelined processor architecture consists of 5 pipeline stages: Instruction Fetch (IF), Instruction Decode and Register Read (ID), Execution or Address Calculation (EX), Data Memory Access (MEM), and Register Write-back (WB). The delay of each stage is summarized below: IF=2 ns, ID=1.5 ns, EX=4 ns, MEM=2.5 ns, WB=2 ns. Which of the following statements are true?
   (a) The maximal attainable clock rate of this processor is 250 MHz.
   (b) All data hazards can be resolved by appropriate data forwarding in this processor design.
   (c) To improve on the clock rate of this processor, the architect decided to add one pipeline stage by splitting the EX stage into two, EX1 and EX2, each having 2 ns delay. Then the maximal attainable clock rate of the new design is 500 MHz.
   (d) Compared with the original 5-stage design, the new 6-stage design tend to have more data hazards.
   (e) None of the above are true.

10. The program below divides two integers through repeated addition and was originally written for a non-pipelined architecture. The divide function takes in as its parameter a pointer to the base of an array of three elements where X is the 1st element at `0($a0)`, Y is the 2nd element at `4($a0)`, and the result Z is to be stored into the 3rd element at `8($a0)`. Line numbers have been added to the left for use in answering the questions below.

```
1  DIVIDE:  add   $t3,$zero,$zero
2           add   $t2,$zero,$zero
3           lw    $t1,4($a0)
4           lw    $t0,0($a0)
5  LOOP:    beq   $t2,$t0,END
6           addi  $t3,$t3,1
7           add   $t2,$t2,$t1
8           j     LOOP
9  END:     sw    $t3,8($a0)
```

If this program is executed on a classical 5-stage (IF-ID-EX-MEM-WB) pipelined processor, then which of the following statements are true?

   (a) If data is forwarded from the pipeline register between MEM and WB of line 4 to EXE of line 5, then data hazard stalls can be avoided for this program.
   (b) If the processor does *not* support data forwarding, then it is impossible for this program to avoid data hazard stalls no matter how we rewrite it.
   (c) If X=6 and Y=3, then the loop will execute 2 times, during which the branch `beq` is taken 1 time and not taken 1 time.
   (d) If X=6 and Y=3, then it takes 14 clock cycles to execute this program on a processor with data-forwarding support.
   (e) None of the above are true.

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