題號: 424

國立臺灣大學106學年度碩士班招生考試試題

科目: 邏輯設計

節次: 7

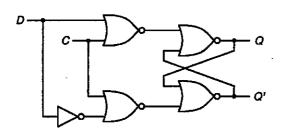
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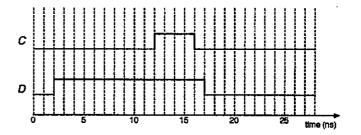
共 1 頁之第 1 頁

※ 注意:全部題目均請作答於試卷內之「非選擇題作答區」, 請標明題號依序作答。

Problem 1 (20%)

Consider the gated D-latch and the timing diagram of C and D below. Show the timing diagram of Q and Q' (for up to 30 ns) assuming that (1) Q = 0 at time 0, and (2) the gate delay is 2 ns for the NOR gate and 1 ns for the inverter.





Problem 2 (20%)

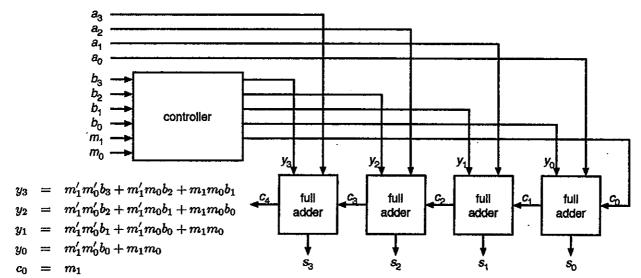
Show the state transition graph of a Moore system whose output is 1 iff three consecutive 0 inputs occurred more recently than three consecutive 1 inputs. A sample input/output trace is given below. Note that you must use the implication table method to reduce the number of states.

Problem 3 (20%)

Using one synchronous 3-bit binary counter with a synchronous clear input, one 3-bit adder, and some extra logic, design a counter that counts the sequence 1, 3, 5, 7, 9.

Problem 4 (20%)

Consider the ALU below where $A = a_3 a_2 a_1 a_0$, $B = b_3 b_2 b_1 b_0$, and $M = m_1 m_0$. What functions (in terms of A and B) does it perform with respect to M = 00, 01, 10, and 11?



Problem 5 (20%)

Consider the equation F(a,b) = (abc + a'b)'.

- 1. Use algebraic manipulation to convert F to the sum of product form. You must show the theorems you use in each step to receive full credits. (8%)
- 2. Implement F by means of an 8-to-1 multiplexer. (6%)
- 3. Implement F by means of a 3-to-8 decoder. (6%)

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