1. (10%) Design the quiescent current of a class AB BJT output stage so that the incremental voltage gain for v_I in the vicinity of the origin is 0.8 V/V for the load equal to 100 Ω. Assume that the BJTs have V_{BE} of 0.7 V at a current of 100 mA and determine the value of V_{BB} required.

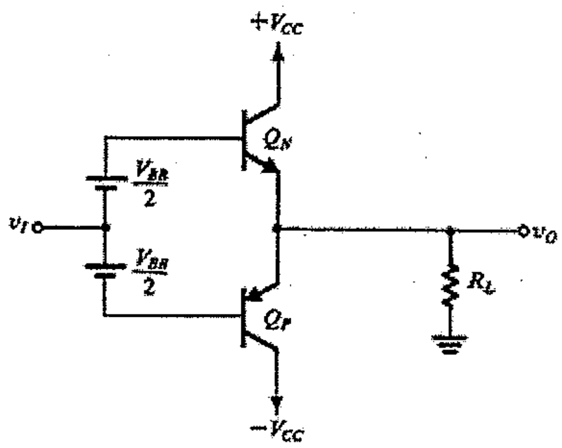

Fig. 1 Class AB output stage

2. (a) (5%) Show that the PSRR⁻ of a CMOS two-stage op amp for which all transistors have the same channel length and are operated at equal $|V_{OV}|$ is given by

$$\text{PSRR}^- = 2\left|\frac{V_A}{V_{OV}}\right|^2$$

(b) (5%) For $|V_{OV}| = 0.2$ V, what is the minimum channel length required to obtain a PSRR⁻ of 80 dB? For the technology available, $|V_A'| = 20$ V/μm.

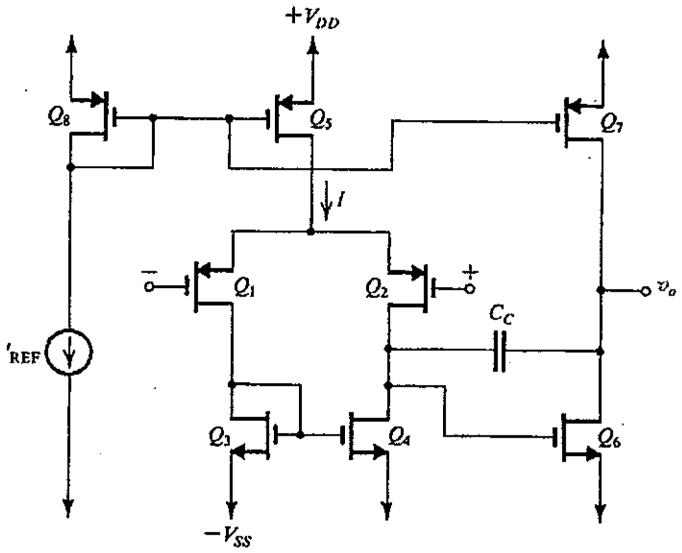

Fig. 2 The basic CMOS two-stage op-amp

3. (a) (5%) Using the fact that for Q ≫ 1 the second-order bandpass response in the neighborhood of ω_0 is the same as the response of a first-order low-pass with 3-dB frequency of $(\omega_0/2Q)$, show that the bandpass response at $\omega = \omega_0 + \delta\omega$, for $\omega \ll \omega_0$, is given by

$$|T(j\omega)| \cong \frac{|T(j\omega_0)|}{\sqrt{1+4Q^2(\delta\omega/\omega_0)^2}}$$

(Hint: first-order low-pass transfer function is $T(s) = \frac{\omega_0}{s+\omega_0}$)

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(b) (5%) Use the relationship derived in (a) together with the 3-dB bandwidth B of the overall amplifier to show that a bandpass amplifier with a 3-dB bandwidth B, designed using N synchronously tuned stages, has an overall transfer function given by

$$|T(j\omega)|_{\text{overall}} = \frac{|T(j\omega_0)|_{\text{overall}}}{\left[1+4\left(2^{1/N}-1\right)\left(\delta\omega/B\right)^2\right]^{N/2}}$$

(Hint: 3-dB bandwidth $B = \frac{\omega_0}{Q}\sqrt{2^{1/N}-1}$)

(c) (3%) Use the relationship derived in (b) to find the attenuation (in decibels) obtained at a bandwidth $2B$ for N = 5. Also find the ratio of the 30-dB bandwidth to the 3-dB bandwidth for N = 5.

(Hint: attenuation function $A(\omega) \equiv -20\log|T(j\omega)|$)

4. (10%) Find the transfer function of the following circuit and determine the value of the half-power frequency.

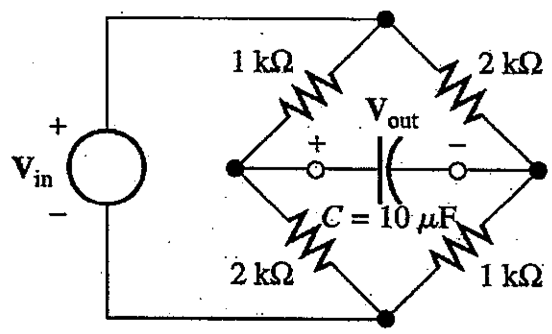

Fig. 3

5. (10%) Assuming that the operational amplifier is almost ideal, what is the output voltage V_{out} for V_{in} = 100 mV, R = 20 ohm.

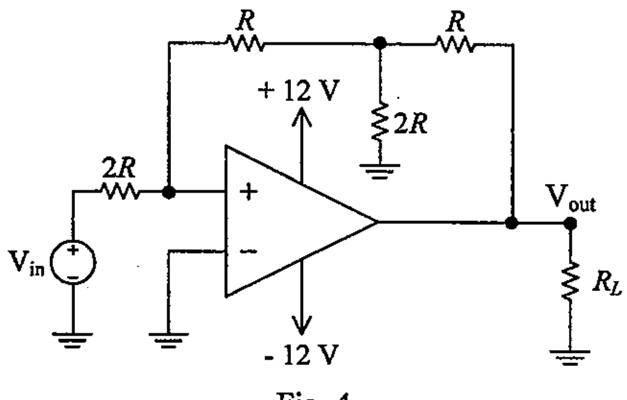

Fig. 4

6. (a) (5%) Draw the schematic diagram of a CMOS inverter and indicate clearly the connection of input, output, supply voltage, and ground to the transistor terminals (including body). (no partial credit will be given)

(b) (8%) Draw the cross-section of physical structure of the above CMOS inverter and show all the transistor terminals. (no partial credit will be given)

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7. In Fig. 5, I_B is 1 mA, R_D = 6 kΩ, R_S = 400 Ω, transistors N_1 and N_2 have W/L = 20μm/0.2μm. Let K_n' = 250 μA/V^2; ignore the channel-length modulation effect. Assume both circuits of Fig. 5(a) and 5(b) are properly biased (V_{CM} is a bias voltage) such that all transistors operate in the saturation region.
(a) (6%) For the circuit shown in Fig. 5(a), find the transistor V_{OV} and g_m, and the voltage gain, V_{out}/V_{id}, of the circuit.
(b) (6%) If you want to double the gain (V_{out}/V_{id}) of the circuit by changing the resistance value of R_S, what value would you adjust R_S?
(c) (6%) The circuit of Fig. 5(a) is modified to a single-ended circuit shown in Fig. 5(b). Find the voltage gain, V_{out}/V_i, of this circuit. Please show your derivations.

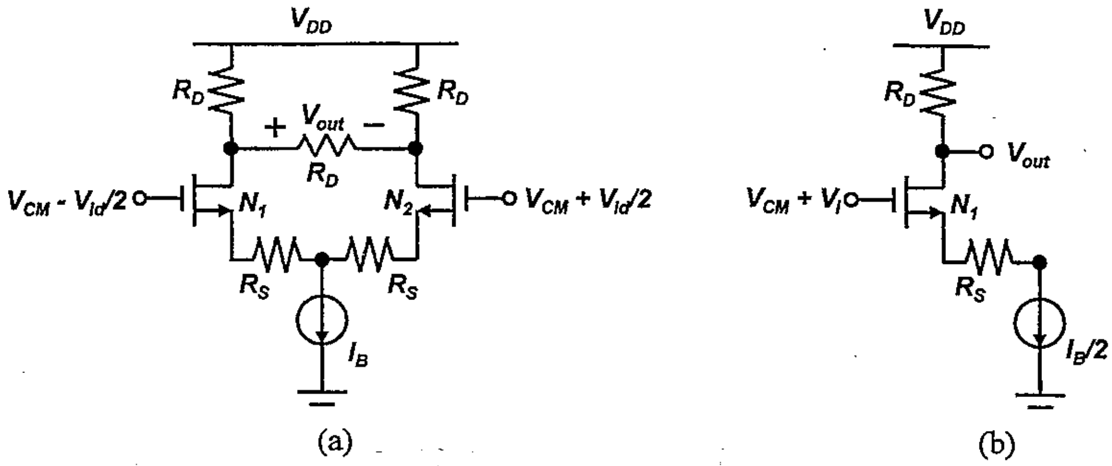

Fig. 5

8. (a) (6%) Fig. 6(a) shows a basing technique to stabilize the drain current (I_D) of a MOS circuit. Explain how this circuit topology helps to stabilize I_D.
(b) (5%) Fig. 6(b) is modified from Fig. 6(a) by removing R_G and connecting the drain and gate terminals together. Can this modified circuit of Fig. 6(b) maintain a stable I_D? Please state your reason.
(c) (5%) Can the circuit of Fig. 6(b) be applied to a common-source amplifier? Please state your reason.

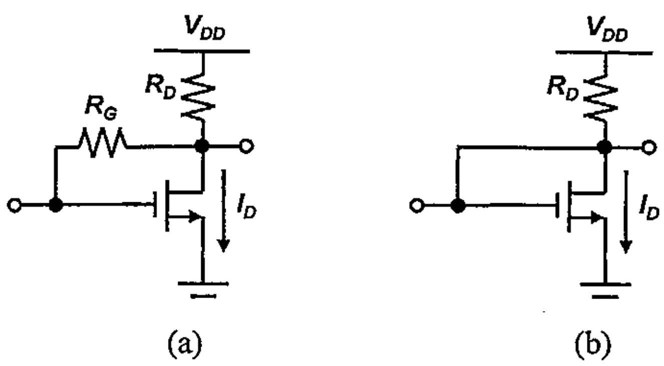

Fig. 6

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