第一及第二大題選擇題考生應作答於『答案卡』(請勿作答於試卷之選擇題作答區)，未作答於答案卡者，本大題不予計分；
非選擇題則請作答於『試卷』之非選擇題作答區。

第一大題：複選題 (每題 5%) － 本大題考生應作答於『答案卡』。

1. What are the approaches to reducing the average memory access time in a computer with memory hierarchy?
(A) reducing the miss rate of cache
(B) using direct mapped cache
(C) increasing the associativity of cache
(D) increasing the cache size

2. What are the features or facts related to a RISC (reduced instruction set computer) architecture?
(A) Instruction format is short and being one size
(B) The MIPS architecture is a RISC machine
(C) The main operations that affect memory are load and store instructions.
(D) A larger register set comprised of most general purpose registers, as compared to CISC (complex Instruction Set Computer) computer
(E) Increase performance through the use of pipelining

3. Which statements are correct?
(A) The slab memory allocation algorithm uses a separate cache for each different object type.
(B) One goal of the buddy memory allocation technique is to solve the external fragmentation problem.
(C) The slab memory allocation algorithm can solve the internal fragmentation problem.
(D) Segmentation fault occurs when a program attempts to access a memory location that it is not allowed to access.

4. Which statements are correct?
(A) Busy waiting is the situation that a process is waiting for an event while it is executing instructions in a loop in the running state.
(B) A spinlock is a lock which causes a thread trying to acquire it using busy waiting.
(C) Rather than busy waiting, the process can block itself. The block operation places a process into a waiting queue and sleep.
(D) Busy waiting is not efficient and does not use anymore in a multiprocessor system.

5. Some factors can influence the performance of GPU kernels. What runtime behaviors that are caused by the kernel code can increase of GPU performance during kernels execution?
(A) Coalesced off-chip memory references
(B) Branch divergence
(C) Non-coalesced off-chip memory references
(D) Use of on-chip memory

6. In an operating system with shared resources, what are necessary conditions for a deadlock to occur?
(A) Resources are required to be mutual exclusive.
(B) Processes are holding some resources and waiting for some resources.
(C) The use of resources can be preempted.
(D) Circular wait conditions occurred between processes
(E) Processes are virtualized

見背面

7. Which of the following scheduling algorithms could result in starvation?
(A) Non-preemptive priority
(B) First-come, first-served
(C) Shortest job first
(D) Round robin
(E) Preemptive Priority

8. What goals can be achieved by the asymmetric encryption algorithm?
(A) Do not subject to the Man-in-the-middle attacks
(B) Authentication: the receiver knows that only the sender could have generated the message.
(C) Secrecy: only the receiver can decrypt the message.
(D) Authentication and secrecy: only the receiver can decrypt the message, and the receiver knows that only the sender could have generated the message.

第二大題：單選題 (每題 5%) -本大題考生應作答於『答案卡』。
9. Which of the following is useful to enhance the performance of a memory management system using demand-paging?
   (A) GPU　　　　　　　(B) instruction cache　　　　(C) data cache
   (D) RISC architecture　　　(E) translation look-ahead buffers

10. We can use semaphores to deal with the n-process mutual exclusion problem. The n processes share a semaphore, called mutex, whose value is initialized to
(A) n　　　　(B) n-1　　　　(C) 2　　　　(D) 1　　　　(E) 0

第三大題：問答題

11. (10%) A microprocessor with CMOS technologies is operating at a frequency F and a voltage V, if we reduce the operating voltage to 0.8V. What percentage will the dynamic energy and dynamic power reduce?

12. (10%) In a pipeline of a microprocessor, state the three types of instructions that would best fill the branch delay slot and explain under what conditions they improve pipeline performance.

13. (10%) A multiprocessor system has four processor cores, each capable of generating 2 loads and 1 store per clock cycle. The processor clock cycle is 2 ns, while the cycle time of the SRAMs used in the memory system is 4 ns. Calculate the minimum number of memory banks required to allow all processors to run at full memory bandwidth.

14. (5%) List the resources required to execute a thread and a process, respectively.

15. (15%) Consider a virtual memory system with a 1 M logical pages with each page 4KByte and 512 MByte of physical memory.
   (a) How many bits in the logical address are needed to address the total logical address?
   (b) How many bits in the logical address are needed to indicate the page number?
   (c) How many bits in the physical address are needed to address the physical memory?
   (d) What is the total size of the page table for a process on this machine, assuming that the page table entry size is 4 Byte?
   (e) What is the benefit if the operating system use a multi-level page tables instead of the one level page table?

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