國立臺灣大學 105 學年度碩士班招生考試試題

1. **(*21%*) Semiconductor physics**
   (a) (1%) In a p-type bulk semiconductor at room temperature, since hole concentration is NOT equal to electron concentration, the entire material is NOT neutral. True or false?
   (b) (3%) Assume in intrinsic Si, the bandgap is 1.1 eV at room temperature, $N_c = 3 \times 10^{19}$ cm^{-3}, and $N_v = 1.5 \times 10^{19}$cm^{-3}, what's the intrinsic carrier concentration?
   (c) (4%) At room temperature, what are *n* (electron density, cm^{-3}) and $E_C - E_F$ (eV) if the semiconductor is doped uniformly with donors of $N_D = 10^{17}$ cm^{-3}? Use $N_c = 3 \times 10^{19}$cm^{-3} for your calculation.
   (d) (4%) Please plot the carrier concentration (with $N_D = 10^{17}$ cm^{-3}) vs. temperature (20 K ~ 800 K).
   (e) (1%) What's the dominant mechanism for current conduction in a semiconductor with non-zero carrier gradient without any external electric field?
   (f) (1%) What's the dominant mechanism for current conduction in a semiconductor with a uniform carrier concentration under non-zero electric field?
   (g) (7%) What are the two major scattering mechanisms for carrier transport in semiconductors? Please make a plot of mobility vs. temperature and explain why.

2. **(*36%*) P/N junction and BJT**
   (a) (5%) Please draw the band diagram of a Si pn junction with non-degenerate doping levels for both p and n regions. Note it's in equilibrium. Label Ec, Ev, Ei, Ef, and depletion region.
   (b) (1%) If you replace Si with Ge for your diode, what do you expect for your turn-on voltage (Si ~ 1.12 eV and Ge ~ 0.66 eV), increase or decrease compared to Si?
   (c) (5%) For an npn BJT (bipolar junction transistor), there exist two "pn junctions" connected via base region. Isn't the same as two "diodes" back-to-back connected? Please argue your answers.
   (d) (8%) Please draw the minority carrier concentration vs. distance (from emitter to base then to collector) for an npn BJT of $N_E > N_B > N_C$ in forward-active mode (i.e. $V_{BE} > 0$ and $V_{BC} < 0$). Please also label the depletion regions and the equilibrium minority carrier levels in all regions. Note: **It's important to consider the effect of different doping concentrations in the emitter, base, and collector regions.**
   (e) (8%) A common-emitter amplifier of a BJT is shown in Fig. 2-1 (p. 2), please draw the small-signal circuit by assuming $C_{C1} \to \infty, C_{C2} \to \infty$, and $C_E \to \infty$.
   (f) (9%) Find R_{in}, R_o, and A_v if $V_{cc} = V_{EE} = 10\,\text{V}$, $V_T = 0.025\,\text{V}$, $V_A = 100\,\text{V}$, $I = 1\,\text{mA}$, $\beta = 100$, $R_c = 8\,\text{k}\Omega$, $R_B = r_o = 100\,\text{k}\Omega$, $R_L = R_{sig} = 5\,\text{k}\Omega$, and $R_e = 223\,\Omega$.

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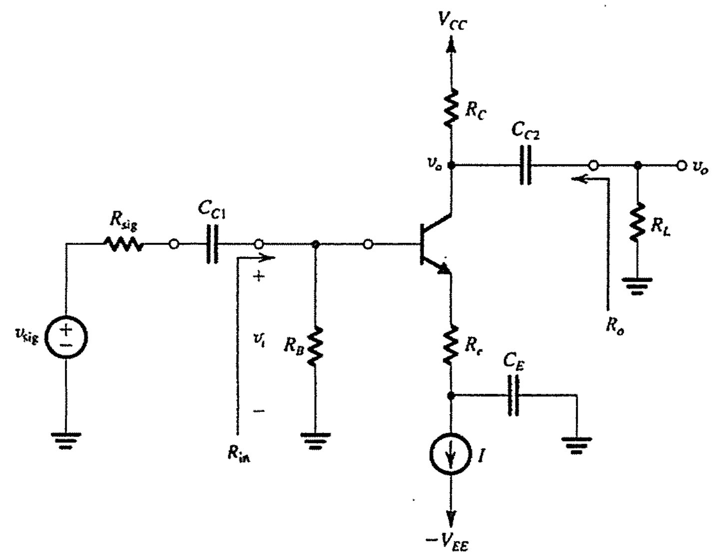

Fig. 2-1

3. ***(43%)* MOSFET**

For a conventional n-type MOSFET, the source and drain are n-type and the substrate is p-type bulk material (Fig. 3-1). Assume no work function difference between metal and substrate (i.e. $V_{FB} = 0$)

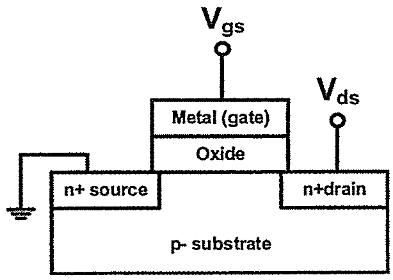

Fig. 3-1

(a) <u>(3%)</u> Please draw the boundary of depletion regions for n-type MOSFET and label the regions if $V_g > V_{th}$ and $V_{ds} > 0$. Note: <u>**Re-plot the figure in your answer sheet.**</u>

(b) <u>(4%)</u> If we apply a positive gate bias (< V_{th}), the device is OFF and NO current conduction occurs, meaning no carriers (electrons) in the channel. However, based on charge conservation and Gauss' law, where are the missing negative charges and what are they?

(c) <u>(4%)</u> If we replace the substrate type with n-type Si, which is the same as source and drain, but less doping (Fig. 3-2), when the device is OFF ($V_{gs} < V_{th}$), the device has huge leakage current between source and drain. Where is it from? <u>**Please re-plot the device and label the leakage current path on your answer sheet**</u>.

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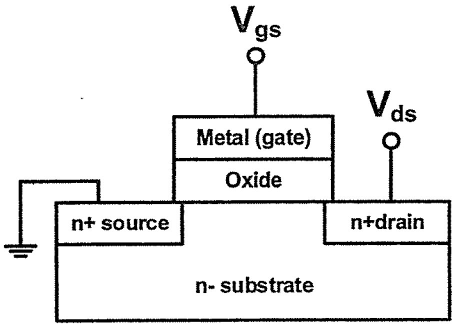

Fig. 3-2

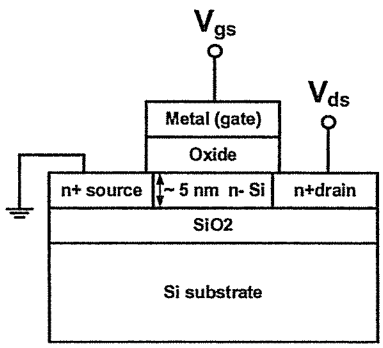

Fig. 3-3

(d) (4%) Following (c), if we use a SOI (silicon on insulator, see Fig. 3-3) as substrate materials with an ultrathin Si layer (~ 5 nm) on top of the oxide, we can reduce the leakage current. Please explain.

(e) (8%) See Fig. 3-4, assume $k_n' = 4k_p' = 400\ \mu A/V^2$ and $V_{tn} = -V_{tp} = 0.4\ V$. As terminals A and B are grounded and the overdrive voltage is 0.2 V, please specify W/L for Q_1, Q_2, Q_3, and Q_4 conducting a drain current of 200 μA. Write down your equations and fill in the values of W/L for different transistors in Table 3-1. **Re-make your Table in your answer sheet.**

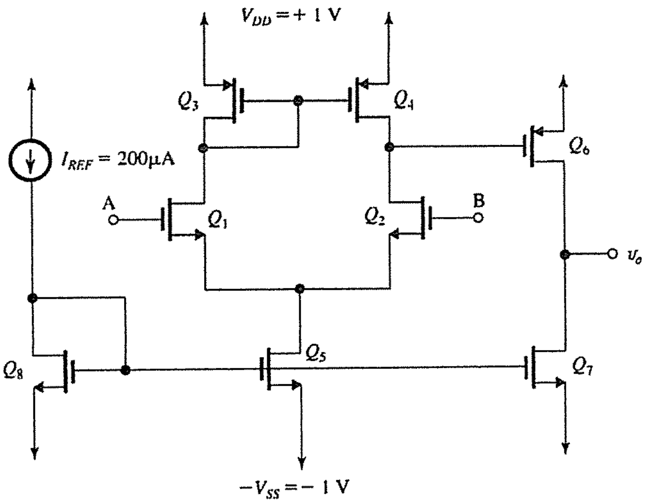

Fig. 3-4

Table 3-1

	$Q_1/Q_2/Q_8$	Q_3/Q_4	Q_5/Q_7	Q_6
W/L				

(f) (6%) Find the common-mode range of input voltage at terminals A and B.

(g) (4%) Find the allowable range of the output voltage (v_o).

(h) (10%) With $v_A = \frac{v_{id}}{2} = -v_B$, find the voltage gain $\frac{v_o}{v_{id}}$. Assume Early voltage is 5 V.