國立臺灣大學 103 學年度碩士班招生考試試題

1. (10%) Convert the number $(54.63)_7$ to binary.

2. (15%)
   (a) (5%) What does the Consensus Theorem in Boolean algebra say? Prove the validity of the theorem.
   (b) (10%) Use the Consensus Theorem and other Boolean algebra properties to minimize the following sum-of-products Boolean expression f, and show your minimization steps.

$$f = ADE' + AD' + A'CE' + A'C'E' + BE + B'C'E + CF + EF'$$

3. (15%) Consider the Boolean function $f(x_1, x_2, x_3, x_4, x_5, x_6)$ over variables x_1, x_2, x_3, x_4, x_5, x_6 with the following (incomplete) function map. Suppose f can be expressed as a conjunction of two functions $g(x_1, x_2, x_3)$ and $h(x_4, x_5, x_6)$, i.e., $f = g \cdot h$.
   (a) (5%) How many solutions are there to function f?
   (b) (5%) How many solutions are there to the function pair (g, h)?
   (c) (5%) Show one solution to (g, h) by expressing g and h with their minterm expansions.

$x_4x_5x_6$ \ $x_1x_2x_3$	000	001	010	011	100	101	110	111
000			0					
001		1						
010							1	
011				1				
100								0
101						0		
110	1							
111					1			

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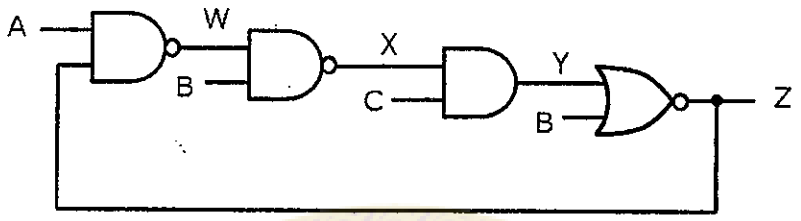
4. (15%) For the circuit given below, assume all the gates have propagation delay 1 ns.



(a) (5%) Show the truth table of function Z in terms of input variables A, B, and C.

(b) (5%) Can a static 1-hazard happen in Z? If yes, under what condition (that is, fixing A, B, C to certain values for enough time and then switching one of the inputs to its opposite value) can it happen?

(c) (5%) Assume the inputs A, B, C and output Z of the circuit are to be connected to D Flip-Flops, which have setup time 1 ns and propagation delay 0 ns. What is the minimal clock cycle under which the circuit can operate correctly?

5. (20%)

(a) (10%) Show an FSM example where row matching cannot reduce the number of states to its minimum. (*Row matching* iteratively merges two equivalent states which have the same next state and output for every input.)

(b) (10%) Prove or disprove that row matching is exact for the state reduction of FSMs corresponding to sequence detectors that reset after every k inputs for some constant $k \geq 1$.

6. (25%) Consider the following block diagram (consisting of a combinational circuit, a control circuit, shift registers, and D Flip-Flops), where "*St*" is the start signal of the controller input, "*Load*" the load signal of the controller output, "*Sh*" the shift signal of the controller output, "*Done*" the finish signal of the controller output, "SI" the serial data input of shift-registers, "Clr" asynchronous clear of the Flip-Flops, "CE" the clock enable signal of Flip-Flops. Assume all clock pins are driven by the same clock signal and the two shift-registers have the parallel input loading capability. The circuit compares two 4-bit integers $A = (a_0, a_1, a_2, a_3)$ and $B = (b_0, b_1, b_2, b_3)$ in **2's complement**, and sorts them by

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placing the larger number in the upper shift-register and placing the smaller one in the lower shift-register. (Assume a_3 and b_3 are the most significant bits of A and B, respectively.)

(a) (15 %) Show the state table of the combinational circuit by denoting the states as S_0, S_1, etc.

(b) (10 %) Draw the state transition graph of the control circuit. (Assume that the start signal St automatically returns to 0 after one clock cycle.)