※ 注意：請用 2B 鉛筆作答於答案卡，並先詳閱答案卡上之「畫記說明」。

單選題 76% (每題答對得 4 分，未答得 0 分，答錯倒扣 2 分)

1. Pipelining in CPU design is aimed to provide the optimal
   (A) throughput (B) latency (C) space parallelism (D) caching
   of instruction execution.

2. Given a non-pipelined CPU operating at 50 MHz, we are optimizing the CPU with a 4-stage pipeline
   design. In an ideal case, what is the operating clock frequency for the 4-stage pipeline CPU?
   (A) 50 MHz (B) 100 MHz (C) 150 MHz (D) 200 MHz (E) 400 MHz

3. Direct Memory Access (DMA) is
   (A) worse (B) better (C) the same
   in performance for small transfers than interrupt driven I/O.

4. Suppose a 32-bit CPU with physical address bus $A_{31}A_{30} ..... A_1 A_0$ and assume that the data cache has
   the following structure:

   > Cache structure is set associative with 2 lots per set
   > Cache size is 128 KBytes
   > Cache block size is 16 Bytes and a word is 32-bit (4 Bytes)
   > Cache is indexed with physical address

   The address bits
   (A) $A_{16}A_{15}...A_4$　(B) $A_{15}A_{15}...A_4$　(C) $A_{14}A_{15}...A_4$　(D) $A_{13}A_{15}...A_4$　(E) $A_{13}A_{15}...A_3$
   are used as index address for the cache.

5. Suppose a 32-bit CPU with physical address bus $A_{31}A_{30} ..... A_1 A_0$ and assume that the data cache has
   the following structure:

   > Cache structure is direct-mapped
   > Cache size is 128 KBytes
   > Cache block size is 16 Bytes and a word is 32-bit (4 Bytes)
   > Cache is indexed with physical address

   The address bits
   (A) $A_{16}A_{15}...A_4$ (B) $A_{15}A_{15}...A_4$　(C) $A_{14}A_{15}...A_4$ (D) $A_{13}A_{15}...A_4$ (E) $A_{13}A_{15}...A_3$
   are used as index address for the cache.

6. A program is compiled into 10 billion instructions and is to be executed by a 5-stage pipelined CPU with
   1 GHz clocks. Each instruction results in an average of 2.2 stall cycles. What is the execution time for
   this application?
   (A) 42 (B) 32 (C) 22 (D) 4.4 (E) 6.4
   seconds.

7. What instruction in ARM processors does not affect the conditional code?
   (A) ADDS r0,r1,r2　(B) ADD r0,r1,r2　(C) CMP r1,r2　(D) TST r1,r2

8. In a paged virtual memory system,
   (A) threading (B) thrashing (C) signaling (D) segmentation (E) stacking
   is a condition in which excessive paging operations are taking place.

9. In a segmentation virtual memory system,
   (A) internal fragmentation (B) external fragmentation (C) threading (D) thrashing (E) signaling
   occurs if holes left in physical memory when segments are destroyed.

10. What allocation method is used in Microsoft FAT file systems?

見背面

(A) continuous (B) indexed (C) linked (D) hashed (E) paged
allocation.

11. What allocation method is used in Linux ext2 or ext3 file systems?
    (A) continuous (B) indexed (C) linked (D) hashed (E) paged
    allocation.

12. Transport Layer Security (TLS) uses
    (A) asymmetric cryptography (B) symmetric cryptography (C) message authentication codes (MAC)
    (D) one-way hash functions (E) bloom filters
    for key exchange.

13. What locking mechanism is better suited for multiprocessor where threads run for a short period of time?
    (A) spinlocks (B) mutexes (C) semaphores (D) adaptive mutexes (E) condition variables.

14. In Linux or Windows, a device driver needing the best performance should be run in
    (A) user mode (B) middleware mode (C) kernel mode (D) application mode (E) virtual mode

15. What is the most required hardware support for the synchronization implementation in an operating
    system?
    (A) data cache (B) instruction cache (C) translation look-ahead buffers (D) atomic read-modify-write
    cycle (E) superscalar architecture

16. Which of the scheduling approach should be used in a real-time operating system?
    (A) First Come First Serve　　(B) Shortest-Job First　　(C) Non-preemptive priority　　(D)
    Round-Robin (E) Priority-based preemptive

17. An application spends 80% of its time doing multiply instructions. If the multiplier is sped up by 4 times,
    the application will run
    (A) 5 (B) 4 (C) 3 (D) 2.5 (E) 2
    times faster.

18. An application spends 80% of its time doing multiply instructions. If the multiplier is sped up by infinite
    times, the application will run
    (A) 5 (B) 4 (C) 3 (D) 2.5 (E) 2
    times faster.

19. What statement is wrong?
    (A) Both threads and processes are execution units in an application.
    (B) Processes are independent execution units that contain their own state information, use their own
        address spaces.
    (C) A single process can contain multiple threads
    (D) All threads within a process can communicate with each other directly through global variables.
    (E) Threads in different processes can communicate with each other directly through global variables.

複選題 24% (每題全對得 4 分，部分答對或未作答不給分亦不倒扣)

20. (A) instruction pre-fetch (B) instruction buffer (C) branching (D) cache misses (E) resource constraints
    will keep the pipeline from being full.

21. Signals are an inter-process communication mechanism in Unix/Linux OS. Signals can be generated by
    (A) a user shell command
    (B) programs via system calls

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(C) the kernel

(D) an interrupt or exception handler.

22. In UNIX/Linux, inter-process communication (IPC) mechanisms includes

(A) Shared memory segments (B) Semaphores (C) Message queues (D) Signals (E) Pipes.

23. In a system with shared resources, which are necessary conditions for a deadlock to occur?

(A) Mutual exclusion uses of resources.

(B) Processes are holding some resources and waiting for some resources.

(C) The uses of resources can be preempted.

(D) Circular wait conditions occurred between processes.

(E) The uses of resources cannot be preempted.

24. Features that are typically found in RISC architectures include:

(A) large number of registers

(B) uniform instruction format

(C) load-store operations

(D) hardwired control unit

(E) arithmetic instructions directly operating on memory data

25. If we run the following program on a 32-bit machine, what outputs might be generated?

```
#include <stdio.h>
int main()
{
    int A[3]={1,2,3};
    int *ptr;
    ptr=A;
    printf(" %p : %d \n",ptr,*ptr);
    ptr++;
    printf(" %p : %d \n",ptr,*ptr);
    return 0;
}
```

(A) 0xbfe5a870 : 1
0xbfe5a874 : 2

(B) 0xbfe1a5e0 : 1
0xbfe1a5e4 : 2

(C) 0xbfe5a870 : 2
0xbfe5a874 : 3

(D) 0xbfe1a5e0 : 2
0xbfe1a5e4 : 3

(E) 0xbfe5a870 : 1
0xbfe5a874 : 3

試題隨卷繳回