※ 注意：請用 2B 鉛筆作答於答案卡，並先詳閱答案卡上之「畫記說明」。

共23題複選題，每一選項獨立記分，答對一個選項得該題1/5分數，答錯一個選項倒扣該題1/10分數，可扣至負分。例如：如正確答案為abc，若答abd可得3/5-2/10=2/5該題分數，但若答ade則得1/5-4/10=-1/5該題分數。

1. (4%) A computer with a direct-mapped cache has an instruction miss rate of 2% and data miss rate of 1.7%. Suppose the computer has a clock cycle time of 20 ns, and the CPI without memory stall is 2 cycles per instruction. Suppose that the miss penalty is 200 ns, and there is, on average, one memory reference for data every two instructions. How much time, on average, does the computer need to execute a program with 10000 instructions?

   (a) 457 μs.

   (b) 459 μs.

   (c) 461 μs.

   (d) 463 μs.

   (e) None of the above are correct.

2. (4%) A program repeatedly performs a three-step process. It reads in a 4-KB block of data from disk, does some processing on the data, and then writes out the result as another 4-KB block elsewhere on the disk. Each block is contiguous and randomly located on a single track on the disk. The disk drive rotates at 7200 RPM, has an average seek time of 8 ms, and has a transfer rate of 20 MB/sec. The controller overhead is 2 ms. No other programs are using the disk processor, and there is no overlapping of disk operation with processing. The processing step takes 20 million clock cycles, and the clock rate is 400 MHz. What is the overall throughput of the system in blocks processed per second?

   (a) 11.69.

   (b) 12.69.

   (c) 13.69.

   (d) 14.69.

   (e) None of the above are correct.

3. (4%) Assume that on a 2 GHz machine, it takes 1 clock cycle to execute an `add`, `addi`, or `sub` instruction and 2 clock cycles to execute a `beq` or `j` instruction. What is the MIPS achieved by the program below?

```
        add  $t0,$zero,$zero
loop:   beq  $a1,$zero,finish
        add  $t0,$t0,$a0
        sub  $a1,$a1,1
        j    loop
finish: addi $t0,%t0,100
        add  $v0,$t0,$zero
```

   (a) 1342

   (b) 1344

   (c) 1346

   (d) 1348

   (e) None of the above are correct.

4. (4%) Consider a paging system with in-memory page tables. Suppose that a memory reference takes 100 nanoseconds, while a TLB (translation look-aside buffer) access takes 5 nanoseconds. If the effective memory-access time is x nanoseconds when the TLB hit rate is 90%, and y nanoseconds when the TLB hit rate is 70%. What is $[\log_2(x-y)]$?

   (a) 3

   (b) 4

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(c) 5

(d) 6

(e) None of the above are correct.

5. (6%) For two processes on the same machine to communicate with each other, which of the following mechanisms do *not* require any kernel intervention at all?

   (a) Message passing.

   (b) Remote procedure call.

   (c) Shared memory.

   (d) TCP/IP socket.

   (e) All of the above require some kernel intervention.

6. (4%) Forwarding is a common technique to eliminate data hazards occurring among pipelining instructions. However, not all data hazards can be eliminated by forwarding. Suppose on a particular machine, if an instruction following a `load` instruction depends on the results of the `load` instruction, then a data hazard has occurred, and the pipeline is stalled for one cycle. Which of the following statements are *not* correct?

   (a) In addition to data hazards, there can be control hazards in this situation because we can not determine the proper data to load in the MEM pipeline stage.

   (b) Assume the percentage of `load` instruction is 20% in a program, and half the time the instruction following a `load` needs the results of the `load` instruction. Then the performance degradation due to the data hazard is 1.1.

   (c) Instruction scheduling can be used to eliminate this kind of data hazards.

   (d) Instruction scheduling does not have any run-time overhead, as it is done at compile time by the compiler; however, it usually increases compilation time because the compiler needs to perform some extra work.

   (e) All of the above are correct.

7. (4%) Protecting the operating system is crucial to ensuring that the computer system operates correctly. Provision of this protection is the reason behind dual-mode operation, memory protection, and the timer. To allow maximum flexibility, however, we would also like to place minimal constraints on the user. The following is a list of operations that are normally protected.

   - Change to user mode (cu).
   - Change to kernel mode (ck).
   - Read from kernel memory (rk).
   - Write into kernel memory (wk).
   - Fetch an instruction from kernel memory (fk).
   - Turn on timer interrupt (t1).
   - Turn off timer interrupt (t0).

   What is the minimal set of instructions that must be protected?

   (a) {ck, rk, wk, t0}.

   (b) {ck, wk, fk, t0}.

   (c) {ck, wk, t0}.

   (d) {ck, wk}.

   (e) None of the above are correct.

8. (6%) Suppose there are two possible strategies for improving the performance of a hypothetical machine. We can either make multiplication instructions run four times faster, or we can make memory-access instructions run two times faster. Suppose the benchmark program we use spends 20% of its execution time in multiplication instructions, 50% in memory access, and the rest 30% in other instructions. Which of the following statements are *not* correct?

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(a) If we improve multiplication instructions alone, then the speed-up is 1.176.

(b) If we improve memory-access instructions alone, then the speed-up is 1.333.

(c) If we improve both multiplication and memory-access instructions, then the speed-up is 1.667.

(d) The second strategy (making memory-access instructions two times faster) is always more effective as long as the original benchmark program spends 50% or more time in memory-access instructions.

(e) All of the above are correct.

9. (4%) The banker's algorithm can be used for deadlock avoidance. For a system with n processes and m types of resources, what is the order of complexity of this algorithm?

(a) m

(b) n

(c) m^2n

(d) mn^2

(e) None of the above are correct.

10. (4%) Two compilers are being tested for a 2.5 GHz machine with three different classes of instructions: Class A, Class B, and Class C, which require one, two, and three cycles, respectively. Both compilers are used to produce code for a large piece of software. The first compiler's code uses 5 billion Class A instructions, 2 billion Class B instructions, and 1 billion Class C instructions. The second compiler's code uses 10 billion Class A instructions, 1 billion Class B instructions, and 1 billion Class C instructions. Which of the following statements are *not* correct?

(a) Compiler 1's code is slower than compiler 2's in terms of MIPS.

(b) Compiler 1's code is faster than compiler 2's in terms of execution time.

(c) Compiler 1's code has a CPI of 1.5 cycles per instruction.

(d) Compiler 2's code has a CPI of 1.25 cycles per instruction.

(e) All of the above are correct.

11. (4%) What is the value in `$v0` after the execution of the program below?

```
        add  $a0,$zero,3
        add  $a1,$zero,20
        add  $t0,$zero,$zero
loop:   beq  $a1,$zero,finish
        add  $t0,$t0,$a0
        sub  $a1,$a1,1
        j    loop
finish: addi $t0,%t0,100
        add  $v0,$t0,$zero
```

(a) 157

(b) 160

(c) 163

(d) 166

(e) None of the above are correct.

12. (4%) Which of the following actions can help alleviate a thrashing system?

(a) Increase the degree of multiprogramming.

(b) Increase the scheduling quantum of the process with the highest page fault frequency.

(c) Increase the size of paging disk.

(d) Increase the working set size of the process with the highest page fault frequency.

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(e) None of the above can help.

13. (4%) Which of the following are *not* defined in the POSIX standard?

(a) Console commands.
(b) Device drivers.
(c) Library functions.
(d) System calls.
(e) All of the above are defined in POSIX.

14. (4%) Which of the following information are normally *not* included in a process control block (PCB)?

(a) CPU-scheduling information.
(b) I/O device queues.
(c) Memory-management information.
(d) Process identifier.
(e) All of the above are normally included in a PCB.

15. (4%) Which of the following operations are usually *not* involved when an interrupt occurs?

(a) Program counter saved.
(b) New program counter loaded from interrupt service table.
(c) Registers saved and new stack set up.
(d) Service process executed.
(e) All of the above are involved.

16. (6%) Which of the following sequences can *not* be the output when the following two processes are executed concurrently?

```
M=0;

Process 1:
  wait(S);
  printf("11\n");
  signal(S);
  printf("12\n");
  signal(M);

Process 2:
  wait(S);
  printf("21\n");
  signal(S);
  wait(M);
  printf("22\n");
```

(a) 11 → 12 → 21 → 22
(b) 11 → 21 → 12 → 22
(c) 21 → 11 → 12 → 22
(d) 11 → 21 → 22 → 12
(e) Any of the above can be an output.

17. (4%) Which of the following statements about a facility that is to provide support for mutual exclusion are *not* correct?

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(a) A process that halts in its non-critical section must do so without interfering with other processes.

(b) It must not be feasible for a process requiring access to a critical section to be delayed indefinitely.

(c) Some assumptions can be made about relative process speeds or number of processes.

(d) When no process is in a critical section, any process that requests entry to its critical section must be permitted to enter without delay.

(e) All of the above are correct.

18. (4%) Which of the following statements about caches are *not* correct?

(a) A one-way set associative cache performs the same as a direct-mapped cache.

(b) Split cache applies parallel caches to improve cache speed.

(c) Translation look-aside buffer (TLB) is a cache for page table and can help accessing virtual memory faster.

(d) Write-through caches have better consistency between main memory and cache.

(e) All of the above are correct.

19. (4%) Which of the following statements about garbage collection are correct?

(a) A hardware support for garbage collection with Java processors can help the performance of a Java environment.

(b) An advantage is that garbage collection does not consume extra computing resources in deciding which memory to free.

(c) The following mainstream programming languages all provide built-in garbage collection: C, C++, Python, and Ruby.

(d) There can be no memory leaks in a programming language with built-in garbage collection.

(e) None of the above are correct.

20. (4%) Which of the following statements about process scheduling are *not* correct?

(a) Even though a process has been receiving occasional service, it is making only nominal progress; in this case, estimated run time to completion is the most appropriate scheduling criteria.

(b) How often a process voluntarily gives up the CPU for I/O before its quantum expires is an appropriate scheduling criteria if we wish to balance between batch and interactive processes.

(c) In a real-time spacecraft monitoring system, the computer must respond immediately to signals received from the spacecraft; in this case, response time for urgent tasks is the most appropriate scheduling criteria.

(d) In some cases, accumulated wait time is an appropriate scheduling criteria if we wish to minimize the time wasted on waiting.

(e) All of the above are correct.

21. (4%) Which of the following statements about segmented virtual memory are *not* correct?

(a) An advantage is being able to provide protection on a per-segment basis.

(b) Generally speaking, if the average segment size is small, then external fragmentation will also be small.

(c) Memory is structured into multiple spaces, as opposed to a single large vector.

(d) Unlike paging, segmentation can be made visible to user processes.

(e) All of the above are correct.

22. (6%) Which of the following statements about the IEEE single-precision floating point computer numbering format are *not* correct?

(a) There are 1 bit in sign, 8 bits in exponent, and 24 bits in mantissa.

(b) If sign = 0, exponent = 01111101_2, and significand = $01000000000000000000000_2$, then the number represented is 0.3125.

(c) The largest positive number that can be represented is $2(1 - 2^{-24}) \times 2^{127}$.

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(d) The smallest positive number that can be represented is 1×2^{-126}.

(e) All of the above are correct.

23. (4%) Which of the following statements are correct?

```
 1 waiting[i]=1;
 2 key=1;
 3 while (waiting[i] && key) {
 4   key=test_and_set(lock);
 5 }
 6 waiting[i]=0;
 7 j=(i+1)%n;
 8 while ((j!=i) && (!waiting[j])) {
 9   j=(j+1)%n;
10 }
11 if (j==i) {
12   lock=0;
13 }
14 else {
15   waiting[j]=0;
16 }
```

(a) Line 1 can be removed without affecting the correctness of the program.

(b) Line 6 can be removed without affecting the correctness of the program.

(c) The program correctly implements a critical section because it satisfies the mutual-exclusion, progress, and bounded-waiting conditions.

(d) The program correctly implements a critical section using an array of semaphores to avoid busy waiting.

(e) None of the above are correct.

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