

※ 注意：請標明題號依序作答。

1. (25%) For $t < 0$, the circuit shown in Figure 1 is at DC steady state. Assume $V_{S1} = 27\text{ V}$, $V_{S2} = 12\text{ V}$, $R = 200\ \Omega$, $L = 20\text{ mH}$, and $C = 0.1\ \mu\text{F}$. If the switch is thrown at $t = 0$,
 - (a) (6%) Determine if the circuit is underdamped or overdamped for $t > 0$.
 - (b) (5%) Find the capacitor voltage v_C at $t = 0$ and at $t \rightarrow \infty$, respectively.
 - (c) (8%) Find the capacitor voltage $v_C(t)$ at $t > 0$.
 - (d) (6%) What is the minimum capacitor voltage $v_{C,\min}$ at $t > 0$?

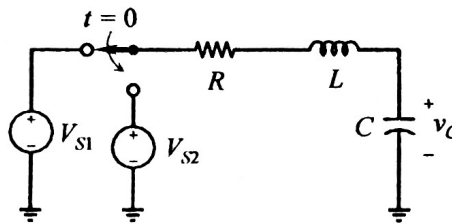


Figure 1

2. (15%) For the filter circuit shown in Figure 2:

Assume $R_1 = 4.7\text{ k}\Omega$, $R_2 = 7.5\text{ k}\Omega$, $L = 4\text{ mH}$, and $C = 0.33\text{ nF}$.

 - (a) (5%) Determine if this circuit is a low-pass, high-pass, bandpass, or handstop filter.
 - (b) (10%) Compute the frequency response function and determine $|V_o / V_i|$ at $\omega = 10^6\text{ rad/s}$.

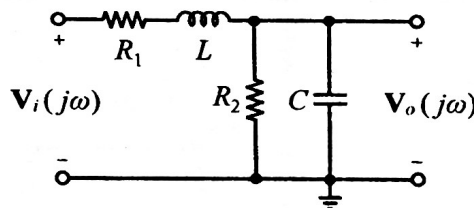


Figure 2

3. (20%) A wave rectifier is shown in the circuit of Figure 3. Assume that a step-down transformer supplies 15 V rms to the rectifier.
 - (a) (6%) If the diodes have an offset voltage of 0.7 V , sketch the input source voltage $v_S(t)$ and the output voltage $v_o(t)$, and state which diodes are on and which are off in the appropriate cycles of $v_S(t)$. The frequency of the source is 60 Hz .
 - (b) (7%) If $R_L = 2.2\text{ k}\Omega$ and a filtering capacitor has a value of $2.5\ \mu\text{F}$, sketch the output voltage $v_o(t)$.
 - (c) (7%) Repeat (b), with the capacitance equal to $100\ \mu\text{F}$.

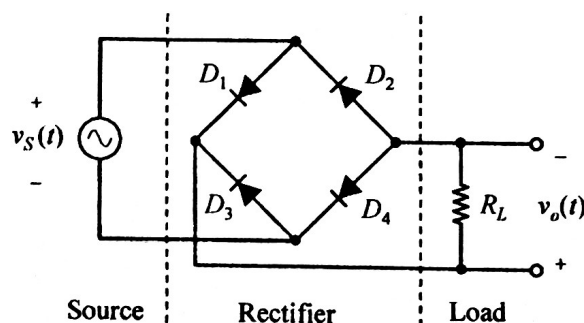


Figure 3

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4. (20%) For the given source voltages v_{s1} and v_{s2} of the circuit shown in Figure 4, please determine the output voltage v_o as a function of time and plot it. Assume ideal operational amplifiers are used. $R_{S1} = R_{S2} = R_{F1} = R_{F2} = R_o = 4 \text{ k}\Omega$ and $C = 250 \mu\text{F}$.

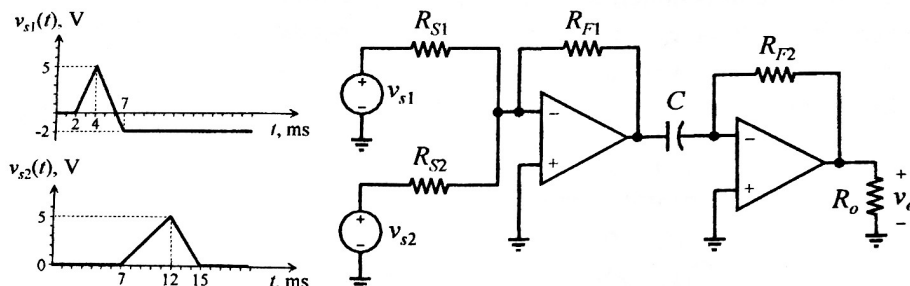


Figure 4

5. (20%) The circuit shown in Figure 5 is similar to a common collector implemented with an *npn* silicon transistor and a single DC supply $V_{CC} = 15 \text{ V}$. v_S is a small sine wave signal with average value of V_{DC} . If $R_1 = 12 \text{ k}\Omega$, $R_2 = 8 \text{ k}\Omega$, $R_C = 50 \Omega$, $R_E = 250 \Omega$ and $C_b = \infty$,
- (7%) Determine the voltage across the collector and emitter, V_{CE} at the operating point Q of the transistor.
 - (7%) Find the voltage gain v_o/v_{in} .
 - (6%) Find the current gain i_o/i_{in}

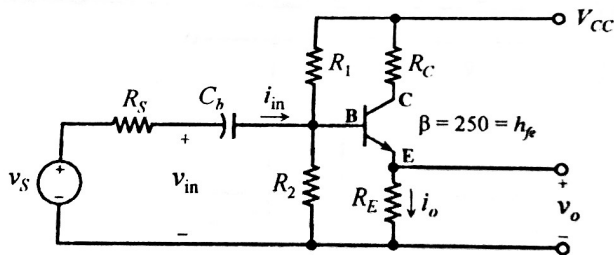


Figure 5

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