第一大題為複選選擇題，共 10 題，每題 5 分；第二大題為單選選擇題，共 10 題，每題 5 分，請作答於『答案卡』中。 ※ 注意：請用 2B 鉛筆作答於答案卡，並先詳閱答案卡上之「畫記說明」。

一、選擇題 (複選) (50%)

1. For a properly-compensated 2-stage amplifier shown in Fig. 1, which of the following(s) is (are) true? (A) The dominate pole is at the output of the second stage. (B) This circuit employs a pole-splitting compensation scheme. (C) The capacitor C_c introduces a zero which leads to additional phase lag. (D) To eliminate systematic dc offset, the transistor sizing should satisfy $(W/L)_6/(W/L)_4 = (W/L)_7/(W/L)_5$.

2. For a Dual-Slope A/D converter shown in Fig. 2, assume V_A is the analog input signal, V_{REF} is a reference voltage. Which of the following(s) is (are) true? (A) The resistor R affects the conversion accuracy. (B) The capacitor C affects the conversion accuracy. (C) The conversion speed is faster than a Flash converter. (D) Switch S_2 is used to discharge capacitor C, setting the initial voltage of V_I to 0.

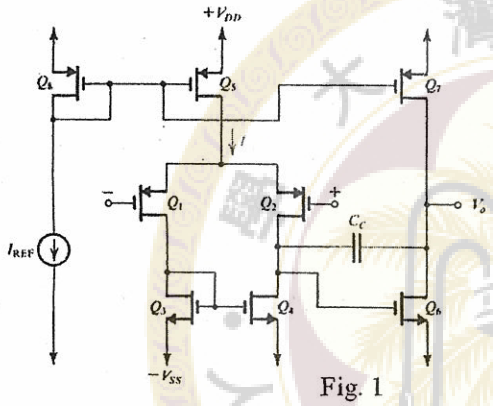

Fig. 1

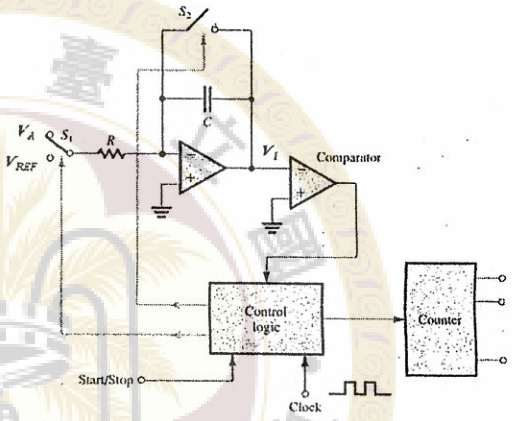

Fig. 2

3. Which of the following(s) regarding the dynamic power dissipation (P_D) of CMOS logic circuits is (are) true? (A) $P_D = fCV_{DD}^2$. (B) $P_D = fCV_{DD}$. (C) In static CMOS logic circuits, P_D is a major part of the total power dissipation. (D) A larger number of fan-out usually leads to a higher P_D.

4. Regarding the logic circuits, which of the following(s) is (are) true? (A) For a sequential circuit, its output depends on the present input and the previous input values. (B) A sequential circuit incorporates memory elements. (C) A monostable circuit can be used as a memory element. (D) A bistable circuit can be used as a memory element.

5. Fig. 3 shows a general architecture of a dynamic logic circuit and its operation timing diagram. Which of the following(s) is (are) true? (A) The output voltage level depends on the transistor sizing. (B) The NM_L (noise margin for low input) is rather low. (C) Domino CMOS logic results in cascadable gates. (D) Charge sharing among internal nodes of the pull-down network (PDN) will not affect the output voltage level.

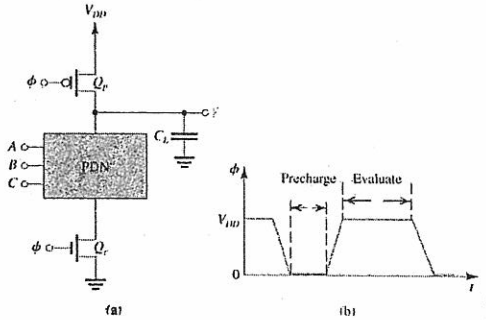

Fig. 3

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6. Fig. 4 shows an integrator circuit. ϕ_1 and ϕ_2 are non-overlapping complementary clocks with a clock period T_c. Which of the following(s) is (are) true? (A) This is an inverting integrator. (B) The integrator time constant is $T_c \times C_1/C_2$. (C) The equivalent resistor of the switched capacitor is $R_{eq}=C_1/T_c$. (D) This integrator is sensitive to stray capacitance.

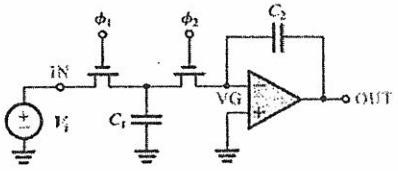

Fig. 4

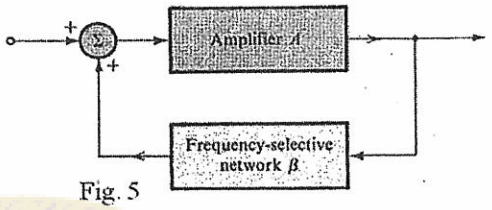

Fig. 5

7. Fig. 5 shows a general positive feedback loop. The loop gain is defined as $L=A\times\beta$. Which of the following(s) is (are) true? (A) To achieve oscillation, L must be 1 for all frequencies. (B) The characteristic equation is $1-L(s) = 0$. (C) The oscillation condition, known as the Barkhausen criterion, states that at a given frequency ω_0, the phase of the loop gain should be π and the magnitude of the loop gain should be unity. (D) To start oscillation, the magnitude of the loop gain should be greater than 1 initially.

8. Which of the following(s) regarding the output stages and power amplifiers is (are) true? (A) Small signal approximations are not applicable. (B) Class-A output stage usually has good efficiency, > 50 %. (C) A typical class-B output stage suffers from cross-over distortion. (D) The conduction angle of class-C amplifier is larger than 180°.

9. Fig. 6(a) and 6(b) are precision rectifiers. Which of the following(s) is (are) true? (A) Both circuits are precision full-wave rectifier. (B) Both circuits have the same v_I-v_O transfer curve. (C) The feedback loops of both circuits are closed all the time (i.e. no open loop operation). (D) In Fig. 6(b), diode D_2 clamps the opamp output to one diode drop below ground as v_O goes negative, and acts as a "catching diode".

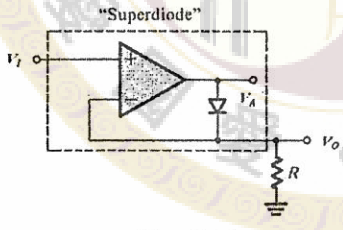

Fig. 6(a)

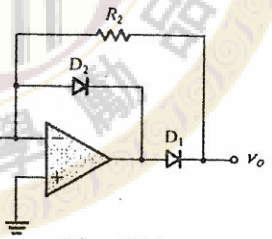

Fig. 6(b)

10. Fig. 7 is a biquad circuit. Which of the following(s) is (are) true? (A) This is a Tow-Thomas biquad. (B) V_1 is a band-pass signal. (C) V_3 is a low-pass signal. (D) High-pass signal is not available in this implementaiton.

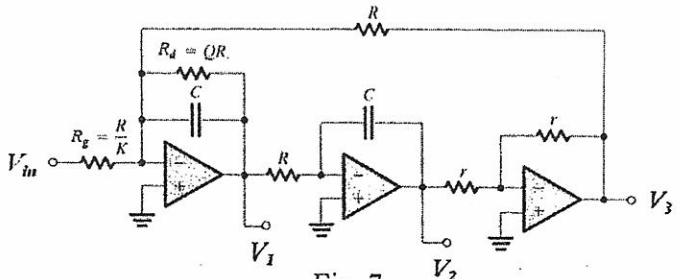

Fig. 7

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二、選擇題 (單選) (50%)

11. For the following circuit (Fig. 8), what is the voltage gain (V_{opt}/V_{input})?
(A) (R2/R1), (B) –(R2/R1), (C) 1+(R2/R1), (D) –(1+(R2/R1)), (E) 1-(R2/R1).

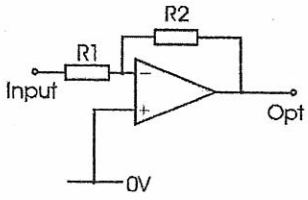

Fig. 8

12. Following the above question, if a capacitor C is added to the cirsuit as shown below (Fig. 9), what is the cutoff frequency, f_0, of such a circuit?
(A) $[(1/R1)+(1/R2)]^{-1}(2\pi C)^{-1}$, (B) $[2\pi (R1+R2) C]^{-1}$, (C) $(2\pi R2 C)^{-1}$, (D) $(2\pi R1 C)^{-1}$, (E) no cutoff frequency.

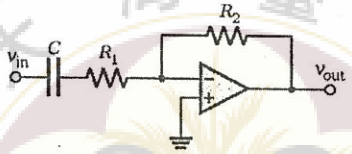

Fig. 9

13. From question 12, the above circuit is
(A) a low pass filter,
(B) a high pass filter,
(C) a band pass filter,
(D) a notch filter,
(E) this is "Not" a filter.

14. Which of the following descriptin on CMOS is wrong?
(A) CMOS is more difficult to fabricate than NMOS.
(B) CMOS is the most widely used of all the IC technologies.
(C) CMOS has low static power consumption.
(D) CMOS uses both p-type and n-type substrates.
(E) CMOS is applied to both digital and analog circuits.

15. For a bipolar junction transistor operated at the common-emitter configuration, which of the following description is wrong?
(A) Early effect is determined by the collector voltage.
(B) The base minority carrier density near the base-emitter interface is higher than that near the base-collector interface.
(C) A thickner base layer results in a higher chance of recombination.
(D) The minority carriers are fully depleted across the collector region.
(E) The depletion region in the base-emitter junction tends to shrink while that in the base-collector junction tends to enlarge.

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16. For the active loaded bipolar differential pair shown below (Fig. 10), what is the differential gain, $v_o/(|v_{B2}-v_{B1}|)$, assuming I=1mA, V_A=160, β=100?
(A) 3200V/V, (B) 2000V/V, (C) 1000V/V, (D) 0.0125V/V, (E) 160V/V.

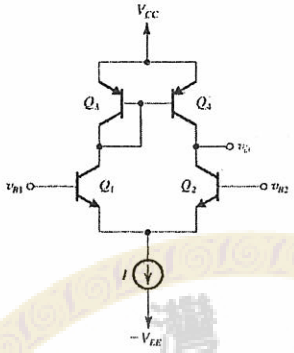

Fig. 10

17. Following the question 16, what is the output impedance?
(A) 125KΩ, (B) 20kΩ, (C) 104kΩ, (D) 160kΩ, (E) 320kΩ.

18. For the description of feedback amplifier structure, which of the following is right?
(A) Shunt-shunt : current-voltage converter, input impedance low, output impedance low.
(B) Shunt-series : curent amplification, , input impedance low, output impedance low.
(C) Series-series : voltage amplification, input impedance high, output impedance high.
(D) Series-shunt : voltage-current converter, input impedance high, output impedance low.
(E) Series-series: current amplification, input impedance high, output impedance low.

19. For a CMOS common-source amplifier with the transfer characteristics (region I, II, III, and IV are labeled in the figure) shown below (Fig. 11), which of the following description is wrong?

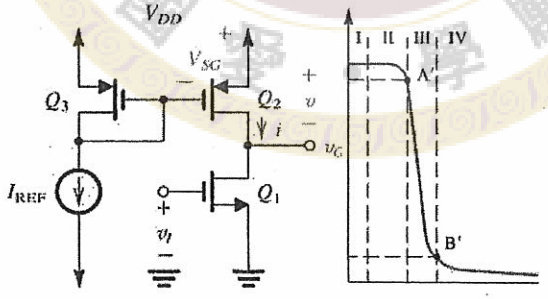

Fig. 11

(A) Region I : Q_2 at cut-off.
(B) Region II: Q_1 in saturation, Q_2 in triode.
(C) Region III: Q_1 and Q_2 in saturation.
(D) Region IV : Q_1 in triode, Q_2 in saturation.
(E) Q_3 and Q_2 form the current mirror.

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20. For the common source amplifier shown below (Fig. 12), the frequency response is determined by external capactiors, C_{in}, C_{out}, and C_s, and the capacitors C_{gs} and C_{gd} in the MOS small signal model. Which of the following description is wrong?
    (A) C_{in} and C_{out} can blcok DC signals at the input and output, respectively.
    (B) C_s is a bypass capacitor acting as a perfect short circuit at all signal frequencies.
    (C) C_{gs} and C_{gd} affect the low frequency band.
    (D) All capacitance can be neglected at midband.
    (E) R_1 and R_2 in the figure determine the bias point of the MOS.

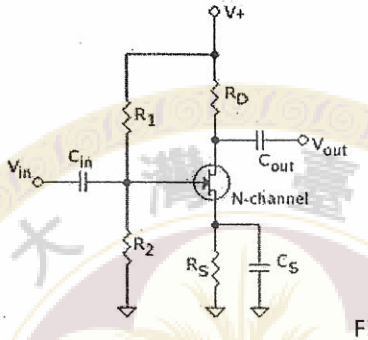

Fig. 12

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