※ 注意：請用 2B 鉛筆作答於答案卡，並先詳閱答案卡上之「畫記說明」。

Multiple Choices (There might be one or more choices in each question. You will get 5% for each question only if all your choices are correct)

1. Which of the following statements are true?

   (a) The input/output units are the devices that allow a computer system to communicate and interact with the outside world as well as store information.

   (b) A disk stores information in units called sectors.

   (c) An I/O controller handles the details of input/output and compensates for any speed differences between I/O devices and other parts of the computer.

   (d) A register is a storage cell that holds the operands of an arithmetic operation and that, when the operation is complete, holds its result.

   (e) The three components of the ALU—the registers, the interconnections between components, and the ALU circuitry—are together called the data path.

2. A processor has a clock rate of 500 MHz, and the following measurements have been made using a simulator.

Instruction class	CPI	Frequency
A	2	40%
B	3	25%
C	3	25%
D	3	10%

   Later the compiler of the processor was improved to enhance the performance. The instruction improvements from this enhanced compiler have been estimated as follows.

Instruction class	Percentage of instructions executed v.s. old compiler
A	90%
B	80%
C	85%
D	90%

   Which of the following statements are true?

   (a) Using the old compiler, the MIPS (million instruction per second) for the processor is 192.3.

   (b) Using the old compiler, the CPI (clock cycle per instruction) of the processor is 2.6.

   (c) Using the enhanced compiler, the CPI for the processor becomes 2.5826.

   (d) Using the enhanced compiler, the processor becomes 1.008 times faster than using the old compiler.

   (e) None of the above statements are true.

3. You are going to enhance a machine, and there are two possible improvements: either make multiply instructions run four times faster than before, or make memory access instructions run two times faster than before. You repeatedly run a program that takes 100 seconds to execute. Of this time, 20% is used for multiplication, 50% for memory access, and 30% for other tasks. Which of the following statements are true?

   (a) The speedup will be 1.176 if you improve only multiplication.

   (b) The speedup will be 1.333 if you improve only the memory access.

   (c) The speedup will be 1.667 if both improvements are made.

   (d) You then repeatedly run a second program that takes 50 seconds to execute. Of this time, 10% is used for multiplication, 15% for memory access, and 75% for other tasks. In this case, you will end up with the same speedup whether you improve only multiplication or only memory access.

   (e) None of the above statements are true.

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4. Consider the following four architecture styles: Accumulator, Memory-Memory, Load-Store, and Stack. Suppose that we are asked to write a sequence of assembly code that implements the C code `a=b+c-d`. Assume:

   - The op code is always 1 byte.
   - All memory addresses are 2 bytes.
   - All data operands are 2 bytes.
   - All instructions are in an integral number of bytes in length.
   - The variables `a`, `b`, `c`, and `d` are initially in memory.
   - For Load-Store architecture, there are 16 general-purpose registers.

   Which of the following statements are true?

   (a) For Accumulator architecture, the length of our sequence of assembly code will be at least 20 bytes.

   (b) For Memory-Memory architecture, the length of our sequence of assembly code will be at least 26 bytes.

   (c) For Load-Store architecture, the length of our sequence of assembly code will be at least 30 bytes.

   (d) For Stack architecture, the length of our sequence of assembly code will be at least 22 bytes.

   (e) None of the above statements are true.

5. Which of the following statements are true?

   (a) For a 16-bit addition, if we use ripple adder and assume that the delay from c_i to c_{i+1} of any full adder is 1 nsec, then the 16-bit addition takes 16 nsec.

   (b) If we use carry-lookahead adder, the 16-bit addition is divided into four 4-bit adders. In each 4-bit adder, there is a 4-bit carry-lookahead circuit. Assume that there is one gate delay for all g_i and p_i, and two gate delays for each carry c_4, c_8, c_{12}, and c_{16}, and finally three gate delays for s_{15}. Then 9 gate delays are required generating c_{16} after X, Y, and c_0 are applied as input.

   (c) Assume that each gate delay requires 0.5 nsec. This 16-bit carry-lookahead adder requires 4.5 nsec for a single addition operation.

   (d) A faster way to apply carry-lookahead circuit is to add a second-level lookahead circuit. With a second-level lookahead circuit, 5 gate delays is required for generating c_{16} after X, Y, and c_0 are applied as input.

   (e) Assume that each gate delay requires 0.5 nsec. This 16-bit carry-lookahead adder requires 2.5 nsec for a single addition operation.

6. Assume that, in MIPS processor, the times required to perform the operations of memory access, ALU operations, and register access are 150 picoseconds (ps), 80 ps, and 50 ps, respectively. And the functions of instruction execution can be divided into 5 units as instruction fetch (IF), decode and register read (ID), ALU operation (EX), data memory access (MEM), and register write back (WB). There are five instruction classes, which are R-type (ALU instructions), load, store, conditional branch, and unconditional jump, and the execution of each instruction class needs to perform part or the whole of the above functional units. Assume the following instruction mix: 30% ALU instruction, 20% load, 20% store, 20% conditional branch, and 10% unconditional jump. Which of the following statements are true?

   (a) Unconditional jump requires the least amount of time to execute because it only uses IF.

   (b) The average execution time per instruction is 480 ps for the single-cycle and fixed clock cycle length implementation approach.

   (c) The average execution time per instruction is 352 ps for the single-cycle but variable-length clock approach, i.e., the length of clock cycle is only as long as the instruction needs to be.

   (d) The average execution time per instruction is 585 ps for the multi-cycle (not pipeline), where each functional unit requires one clock cycle, and fixed clock cycle length approach.

   (e) None of the above statements are true.

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7. Assume that a pipelined processor executes instructions at the throughput of one instruction per clock cycle when no pipeline stalls occur. The pipelined processor executes the subsequent instructions of a jump or branch instructions as if the jump or branch instruction would not change the control flow, until the program counter is overwritten by the jump or branch instruction. The pipelined processor carries out the following operations in the first 3 clock cycles of unconditional jump and conditional branch instruction execution.

   - First cycle: instruction fetch.
   - Second cycle: instruction decode, calculation of the target address, and writing to the program counter if the instruction is a jump.
   - Third cycle: determination of the branch action and writing to the program counter if the instruction is a branch.

   Now, an architect decides to break the instruction fetch into two pipeline cycles. Assume that this action reduces the clock cycle time from 10 ns to 8 ns.

   - 5% of the instruction executed are unconditional jumps;
   - 20% of the instruction executed are conditional branches;
   - 60% of the conditional branches executed turn out to be taken, i.e., the control flow branches to the target address of the branch.

   Which of the following statements are true?

   (a) The new design is 1.1 times faster than the old design.
   (b) The new design is 1.1 times slower than the old design.
   (c) The old design is 1.1 times faster than the new design.
   (d) The old design is 1.1 times slower than the new design.
   (e) None of the above statements are true.

8. Which of the following statements are true for the forwarding unit in a 5-stage pipelined processor?

   (a) The forwarding unit is used to detect the instruction cache stalling.
   (b) The forwarding unit is a sequential circuit which detects the true data dependency for EXE pipeline stage and selects the forwarded results for the execution unit.
   (c) The forwarding unit is a pipeline register which detects the true data dependency for EXE pipeline stage and selects the forwarded results for the execution unit.
   (d) The forwarding unit compares the source register number of the instructions in the MEM and WB stages with the destination register number of the instruction in the decode stage.
   (e) None of the above statements are true.

9. Which of the following statements are true?

   (a) A control hazard is the delay in determining the proper data to load in the MEM stage of a pipelined processor.
   (b) A load-use data hazard occurs because the pipeline flushes the instructions behind.
   (c) To flush instructions in the pipeline means to load the pipeline with the requested instructions using the predicated program counter.
   (d) A branch prediction buffer is a buffer that the compiler uses to predict a branch.
   (e) None of the above statements are true.

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10. Which of the following statements are true for an Intel x86-based PC?
    (a) DMA mechanism can be applied to delegate responsibility from the CPU.
    (b) USB 2.0 is a synchronous bus using handshaking protocol.
    (c) The CPU can fetch and translate IA-32 instructions.
    (d) The CPU can reduce instruction latency with deep pipelining.
    (e) None of the above statements are true.

11. Please choose the criteria in solving the critical section problem in the synchronization of multi-threaded programs from below.
    (a) Bounded waiting
    (b) Turn-around time
    (c) Mutual exclusion
    (d) Progressiveness
    (e) Communication security

12. Please choose the hardware components that are used in operating system designs below.
    (a) TLB
    (b) USB disk
    (c) Mode bit
    (d) Page limit registers
    (e) Interrupt mask register

13. In a multi-processor (distributed computing) system, please select the correct statements from below.
    (a) Push migration and pull migration can happen at the same time in the same system.
    (b) Processor affinity measures the transmission cost between two processors.
    (c) When hard affinity is the policy of the OS, it will never push a task to the backing store.
    (d) NUMA represents "non-uniform memory access."
    (e) Load balancing is only necessary on systems where each processor has its own private ready queue.

14. Assume that we have the following task sets in CPU scheduling.

Process	Burst time	Arrival time
P1	15ms	0ms
P2	47ms	7ms
P3	21ms	25ms

Please select the correct statement from below.

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(a) With FCFS policy, the average waiting time is 15ms.
(b) With preemptive SJF policy, the average waiting time is 10ms.
(c) With non-preemptive SJF policy, the average time is 13ms.
(d) With round-robin policy with quantum size of 3ms, the average response time is 7/3ms.
(e) With round-robin policy with quantum size of 10ms, the average response time is 17/3ms.

15. We are in a transaction scheduling system with three transactions with indices 1, 2, and 3. In addition, we also have three data objects: A, B, and C. The three transactions may read and write the data objects. A read operation by transaction t on object J is denoted R(t,J) while a write operation by t on J is denoted W(t,J). Suppose that we write a transaction schedule from left to right. Please choose the serializable schedules from below.
(a) R(1,A) R(2,A) R(3,A) W(2,B) W(3,B)
(b) R(1,A) W(3,A) R(2,A) W(2,B) W(3,B)
(c) R(3,A) W(2,C) R(3,A) W(2,B) W(1,B)
(d) W(1,C) R(2,A) R(3,C) W(3,B) W(1,B)
(e) R(2,B) W(3,B) R(3,A) R(2,B) R(3,B)

16. Please select the necessary conditions of deadlock from below.
(a) Hold and wait.
(b) Small working set.
(c) Mutual exclusion.
(d) Circular wait.
(e) I/O.

17. In deadlock avoidance, we may use Banker's algorithm to check whether a state is safe or not. Suppose that we have the following matrices.

	Allocation	Max	Available
	A B C D	A B C D	A B C D
P0	1 1 0 0	3 2 6 0	4 1 1 3
P1	0 0 1 2	2 2 3 2	
P2	1 3 2 3	5 3 2 3	
P3	3 0 3 2	4 1 4 3	

Please select the safe sequences from below in this state.
(a) P2 P1 P0 P3
(b) P2 P1 P3 P0
(c) P3 P1 P2 P0
(d) P3 P2 P1 P0
(e) P2 P3 P0 P1

18. Suppose in a demand paging system, we use TLB to speed up the page table lookup. The access time to TLB is 50 nanoseconds while the access time to the main memory is 300 nanoseconds. Please select the correct statements from below.
    (a) At a 90% hit ratio with one-level paging, the effective memory access time is 390 nanoseconds.
    (b) At a 99% hit ratio with one-level paging, the effective memory access time is 356 nanoseconds.
    (c) At a 90% hit ratio with two-level paging, the effective memory access time is 410 nanoseconds.
    (d) At a 99% hit ratio with two-level paging, the effective memory access time is 354 nanoseconds.
    (e) At a 99% hit ratio with three-level paging, the effective memory access time is 359 nanoseconds.

19. Please select from below the techniques that can be used to improve the efficiency of demand paging.
    (a) Backing store separated from user disks.
    (b) Copy-on-write.
    (c) Dirty page checking
    (d) Working set prediction.
    (e) Accurate effective access time calculation.

20. In a disk scheduling system with 100 tracks indexed from zero to 99, we have three track access requests at track 1, 45, and 15 arriving in this sequence. Suppose that the disk head is now at track 24 and moving toward track 99. Please select the correct statements from below.
    (a) With the FCFS policy, the disk head traveling distance for the above three requests is 97.
    (b) With the SSTF policy, the disk head traveling distance for the above three requests is 67.
    (c) With the SCAN policy, the disk head traveling distance for the above three requests is 173.
    (d) With the LOOK policy, the disk head traveling distance for the above three requests is 65.
    (e) With the C-LOOK policy, the disk head traveling distance for the above three requests is 79.