1. (22 pts) Consider the filter circuit in Fig. 1:

(a) (2 pts) What kind of filter function does this circuit realize?

(b) (4 pts) Calculate ω_o and Q of the circuit.

(c) (8 pts) The filter circuit transfer function can be expressed as

$\frac{V_o}{V_i} = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0}$. What are the values of a_2, a_1, a_0, b_1, b_0?

(d) (8 pts) Design a new filter circuit with an additional notch function by adding one more passive component on the original circuit in Fig. 1. Draw the new filter circuit and explain why your design can realize such a notch function. Calculate the corresponding notch frequency ω_n.

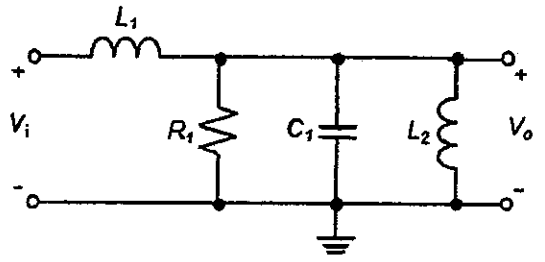

Fig. 1

2. (28 pts) Suppose a standard CMOS inverter in a given technology has a minimum size with $(W/L)_n = n$ and $(W/L)_p = p$, where $p = (\mu_n/\mu_p)\, n = 4n$ for the matched current-driving strength. Assume the area of a gate in this technology can be expressed as $A_{gate} = k \times$ (total NMOS transistor size Σn + total PMOS transistor size Σp). For example, the area of a standard CMOS inverter is equal to $k \times (1n + 1p) = 5kn$.

(a) (4 pts) Design a standard CMOS logic gate to implement the logic function $F = (A + B) \cdot C$. Assume all of the complemented input signals $\bar{A}$, $\bar{B}$, and $\bar{C}$ are also readily available and use as few transistors as possible. Draw the standard CMOS logic design and **size the gate with current-driving capability equal to that of a standard CMOS inverter**. Calculate the corresponding area of the standard CMOS logic gate as a function of k and n.

(b) (8 pts) Design a pseudo-NMOS logic gate to implement the logic function $F = (A + B) \cdot C$. Assume all of the complemented input signals $\bar{A}$, $\bar{B}$, and $\bar{C}$ are also readily available and use as few transistors as possible. Draw the pseudo-NMOS logic design and **size the gate with current-driving capability equal to that of a standard CMOS inverter**. Calculate the corresponding area of the pseudo-NMOS logic gate as a function of k and n. What are the advantage and disadvantage of using pseudo-NMOS logic style to implement this logic function?

(c) (8 pts) Design a dynamic MOS logic gate to implement the logic function $F = (A + B) \cdot C$. Assume all of the complemented input signals $\bar{A}$, $\bar{B}$, and $\bar{C}$ are also readily available and use as few transistors as possible. Draw the dynamic MOS logic design and **size the gate with current-driving capability equal to that of a standard CMOS inverter**. Calculate the corresponding area of the dynamic MOS logic gate as a function of k and n. What are the advantage and disadvantage of using dynamic MOS logic style to implement this logic function?

(d) (8 pts) Design a pass-transistor logic gate to implement the logic function $F = (A + B) \cdot C$. Assume all of the complemented input signals $\bar{A}$, $\bar{B}$, and $\bar{C}$ are also readily available and use as few transistors as possible. Draw the pass-transistor logic design and **size the gate to have minimum gate area**. Calculate the corresponding area of the pass-transistor logic as a function of k and n. What are the advantage and disadvantage of using pass-transistor logic style to implement this logic function?

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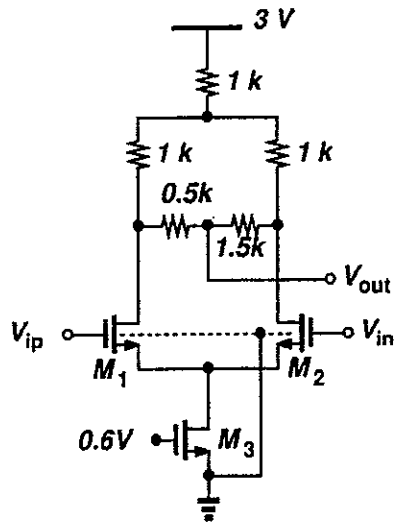
3. (30 pts) For the following differential-to-single circuit, neglect body effect in all transistors for (a)-(c). Channel-length modulation can be neglected in all transistors. Note that $(W/L)_{1,2}$=500/1, $(W/L)3$=4000/1, $\mu_n C_{ox}$=50 μA/V^2, and V_{tn}=0.5V.



(a) (5 pts) First, what is the input common-mode range, V_{icm}, for both transistor M_1-M_3 in saturation region?

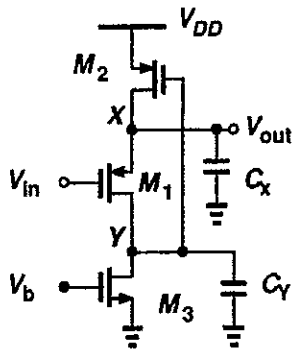
(b) (9 pts) Now, draw the small-signal circuits and derive $V_{out}/\Delta V$. $V_{ip}=V_{icm}+0.5\Delta V$ and $V_{in}=V_{icm}-0.5\Delta V$.

(c) (5 pts) What is PSRR (power-supply rejection ratio)? For this part, you can assume a small voltage perturbation ΔV_{dd} at 3-V power supply, what is the output response?

(d) (6 pts) Let's take body effect into account, where γ=0.3 and $2\phi_f$=0.8. Repeat part (a).

(e) (5 pts) Repeat part (b) with body effect.

4. (20 pts) For the following circuit, neglect body effect in all transistors. Assume all transistors are in saturation region and their associated transconductance and output resistance are $g_{m1,2,3}$ and $r_{o1,2,3}$. To simplify the questions, $r_{o1,2,3}$ are identical and equal to r_o.



(a) (5 pts) First, sketch the transfer curve of V_{out} vs. V_{in}.

(b) (5 pts) Derive the small-signal output resistance (by looking into V_{out}) without considering all capacitors.

(c) (10 pts) Due to negative feedback configuration, please identify the design requirement of the ratio of (C_X / C_Y) to maintain the stability of such circuit, where its phase margin is at least 45 degrees. Please note that C_X and C_Y are all capacitors associated with nodes X and Y.

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