1. (15%) Please analyze the operational circuit shown as Figure 1. Find the output current i_{out} as a function of v_{in}.

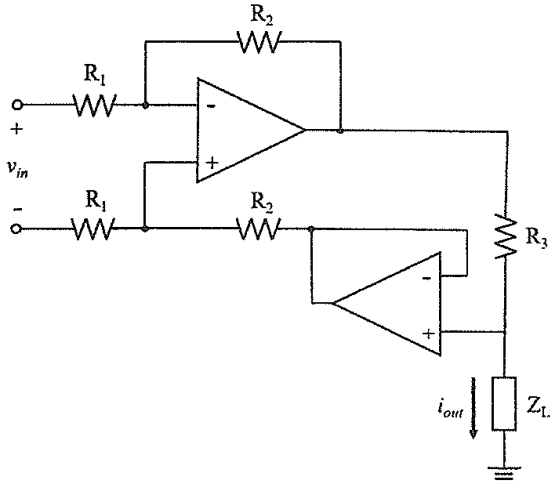

Figure 1

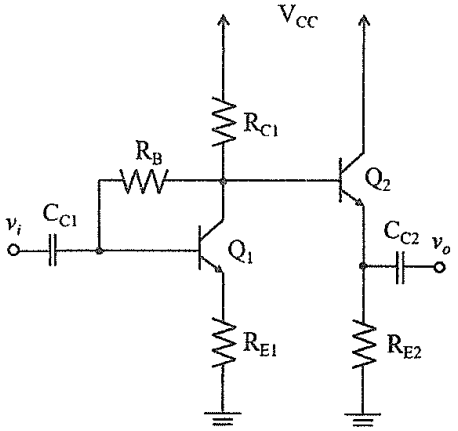

Figure 2

2. (20%) Please analyze the BJT circuit shown in Figure 2. The circuit parameters can be given as V_{CC} = 20 V; R_B = 200 kΩ; R_{C1} = 10 kΩ; R_{E1} = 1 kΩ; R_{E2} = 8 kΩ and β = 50
   (a) (10%) Please find the DC biased current at the collector of Q_1 and Q_2.
   (b) (10%) Please find the small-signal gain of v_o/v_i.

3. (15%) Please analyze the MOSFET circuit shown as Figure 3. Assume all circuit are properly biased and operated in saturation region. Assume the transconductance of NMOS is $g_{m,N}$ and the transconductance of PMOS is $g_{m,P}$. And there is the same finite output resistance (r_o) of these MOSFETs.
   (a) (3%) Please write down the topology of the MOSFET amplifier of each circuit
   (b) (4%) Please derive the small-signal gain of Fig. 3(a)
   (c) (4%) Please derive the small-signal gain of Fig. 3(b)
   (d) (4%) Please derive the small-signal gain of Fig. 3(c)

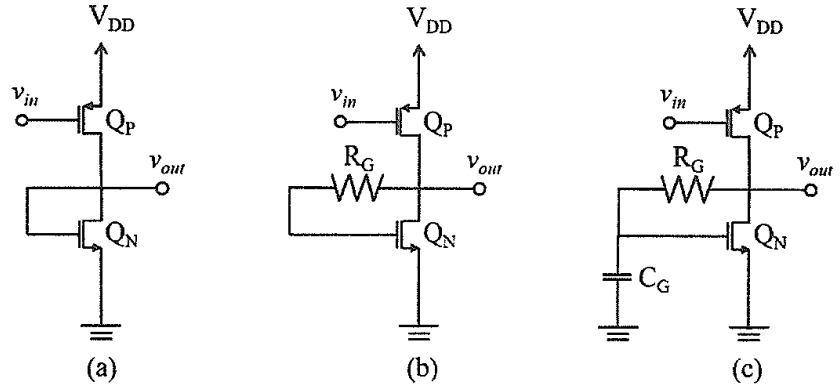

Figure 3

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4. (15%) For a static four-input NAND gate with L = 0.18 μm, all transistor sizes are chosen to match the delay of a basic CMOS inverter with $(W/L)_n = n$ and $(W/L)_p = p$.
   (a) (5%) Please sketch the CMOS circuit for a static four-input NAND gate.
   (b) (6%) For a static four-input NAND gate with $n = 1.5$ and $p = 3$, please give the sizes (W/L) of all transistors.
   (c) (4%) For the static four-input NAND gate, find the ratio of the maximum to minimum current available to (a) charge a load capacitance and (b) discharge a load capacitance.

5. (25%) Design the circuit in Figure 4 to obtain a dc voltage of +0.1 V at each of the drains of Q_1 and Q_2 when $v_{G1} = v_{G2} = 0$ V. Operate all transistors at $V_{OV} = 0.15$V and assume that for the process technology in which the circuit is fabricated, $V_{tn} = 0.4$V and $\mu_n C_{ox} = 400\ \mu A/V^2$. Neglect channel-length modulation.
   (a) (4%) Determine the value of R_D.
   (b) (12%) Determine the W/L ratios of Q_1, Q_2, Q_3, and Q_4.
   (c) (4%) Determine the value of R.
   (d) (5%) What are the lower and upper limits of the input common-mode voltages?

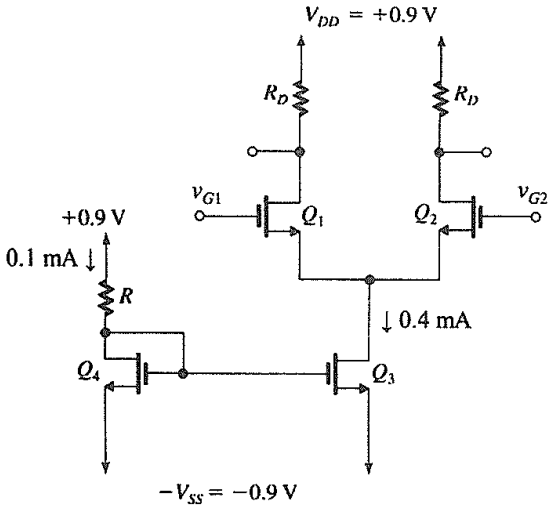

Figure 4

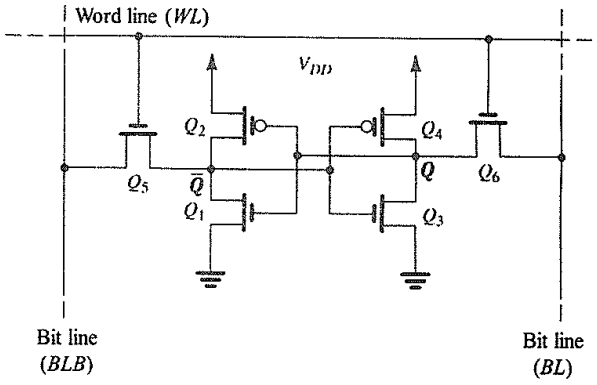

Figure 5

6. (10%) Before the read operation, both bit lines (BL and BLB) are precharged to V_{DD}. Find the maximum allowable $(W/L)_a$ for the access transistors of the SRAM cell shown in Figure 5 so that in a read operation, the voltages at Q and $\overline{Q}$ do not change by more than a threshold voltage $|V_t|$. Assume that the SRAM is fabricated in a 0.18 μm technology for which $V_{DD} = 1.8$ V, $V_{tn} = |V_{tp}| = 0.5$ V and that $(W/L)_n = 1.5$ for pull-down devices.

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