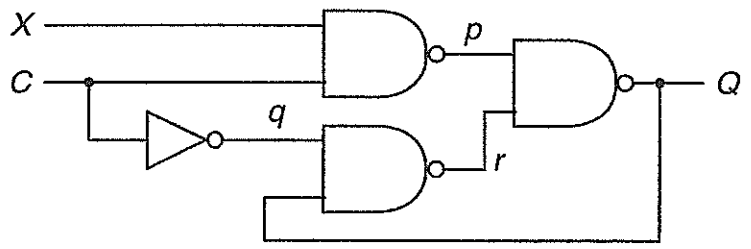
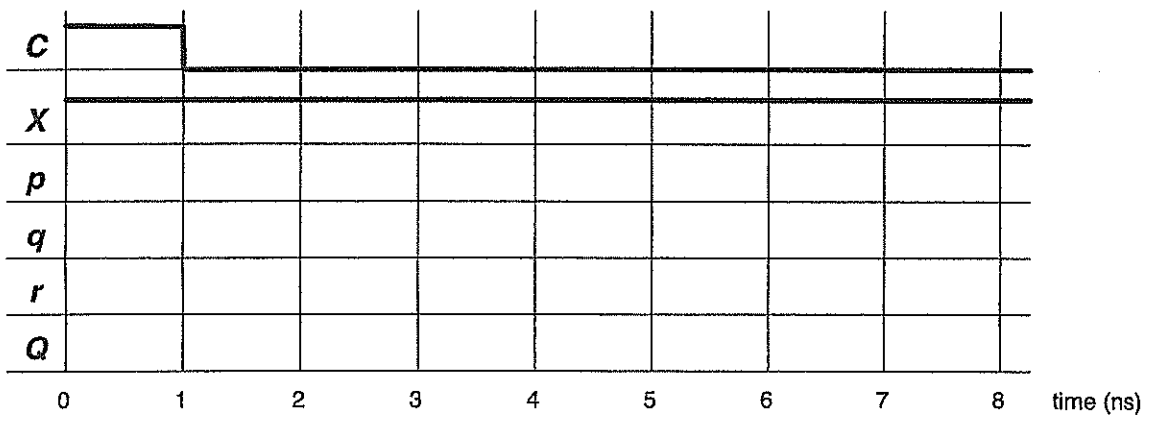
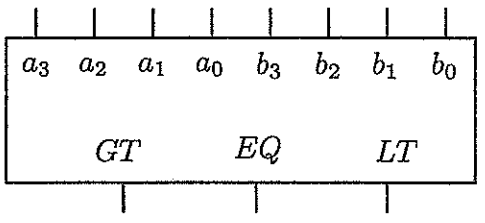
Problem 1 (25%)
Consider the gated *X*-latch below where *X* is the input and *C* the gate input.
(a) What's the next-state equation of the *X*-latch? (5%)
(b) Assume that each gate has a 1 ns delay. Complete the timing diagram below. (10%)
(c) Does the *X*-latch works correctly? If not, fix the problem and justify your solution. (10%)





Problem 2 (20%)
Derive a minimal state table for a single-input and single-output Moore-type FSM that produces an output of 1 if in the input sequence it detects either 110 or 101 patterns. Overlapping sequences should be detected.

Problem 3 (15%)
The 4-bit comparator below compares two binary numbers $A = a_3a_2a_1a_0$ and $B = b_3b_2b_1b_0$ and produces greater than (*GT*), equal (*EQ*), and less than (*LT*) outputs according to the table below. Show how to construct an 8-bit comparator with two 4-bit ones and external logic.



	GT	EQ	LT
A > B	1	0	0
A = B	0	1	0
A < B	0	0	1

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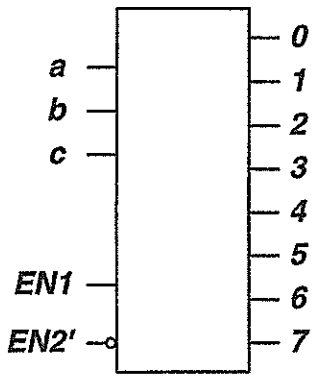
Problem 4 (10%)
Implement the following functions using only two of the decoders described below and two 8-input OR gates.

$$f(w,x,y,z) = \sum m(0,4,5,7,8,12,15)$$

$$g(w,x,y,z) = \sum m(1,3,5,12,13,14)$$



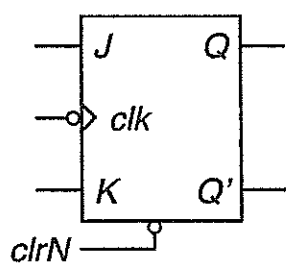
EN1	EN2'	a	b	c	0	1	2	3	4	5	6	7
0	X	X	X	X	0	0	0	0	0	0	0	0
X	1	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	0	1	0	1	0	0	0	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0	0
1	0	0	1	1	0	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	1	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	0	0	0	1	0
1	0	1	1	1	0	0	0	0	0	0	0	1

Problem 5 (15%)
Find **"all"** minimum sum of products expressions for *f* and *g*.

$$f(a,b,c,d) = \sum m(0,2,3,5,7,8,9,10,11) + \sum d(4,15)$$

$$g(a,b,c,d) = \sum m(0,2,4,5,6,7,8,9,10,14) + \sum d(3,13)$$

Problem 6 (15%)
Construct a base 20 **"asynchronous"** counter that counts the number of input pulses (from 0 to 19, back to 0, and repeat) using *JK* flip flops, which, as shown below, are falling-edge triggered and have an active-low clear input, *clrN*. Denote the counter output by $C = C_4C_3C_2C_1C_0$.



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