1. The difference amplifier circuit is shown in Fig. 1.

(a) If v_o can be expressed as $v_o = A_d v_{Id} + A_{cm} v_{Icm}$, where $v_{Id} = v_{I2} - v_{I1}$, $v_{Icm} = \frac{1}{2}(v_{I2} + v_{I1})$. Derive the common-mode gain (A_{cm}) and differential gain (A_d). (10 %)

(b) If $R_2 = R_4 = 2R_1 = 2R_3$, what is the CMRR of the difference amplifier? (5 %)

(c) Assume that the op amp has a dc gain of 80 dB and a 3-dB bandwidth of 100 Hz. Find the 3-dB frequency of the differential gain. (10 %)

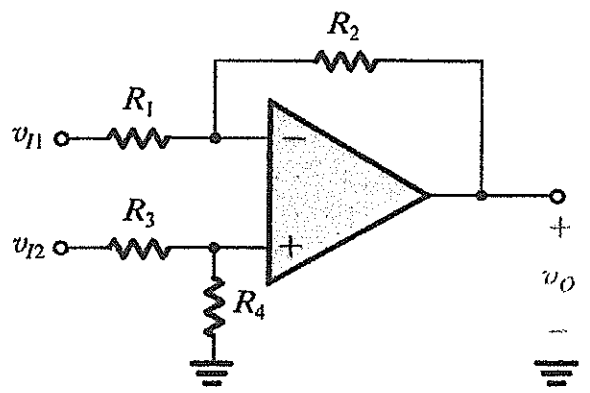

Fig. 1

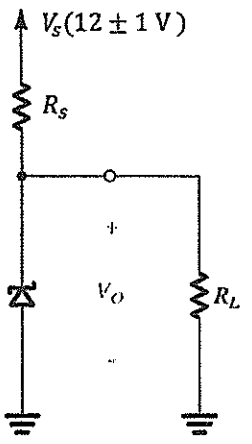

Fig. 2

2. In Fig. 2, the Zener diode is specified to have $V_Z = 8\ V$ at $I_Z = 10\ mA$, $r_Z = 10\ \Omega$, and $I_{ZK} = 0.1\ mA$. The supply voltage is 12 V but can vary $\pm 1\ V$. $R_S = 200\ \Omega$.

(a) If $R_L = 4\ k\Omega$ and V_S is at the nominal value (12 V), find V_O. (5 %)

(b) Find the line regulation of this circuit. (5 %)

(c) Find the load regulation of this circuit. (5 %)

(d) What is the requirement on the value of R_L, for the circuit to operate properly across the possible range of V_S. (5 %)

3. The amplifier circuit is shown in Fig. 3. The two MOSFETs are perfectly matched with $\mu_p C_{ox} \frac{W_2}{L_2} = \mu_n C_{ox} \frac{W_1}{L_1} = 25\mu A/V^2$ and $|V_{tp}| = V_{tn} = 2\ V$.

(a) Please find the DC drain current and drain voltage of Q_1. (5 %)

(b) Draw the small-signal model and find the voltage gain (v_o/v_i). (10 %)

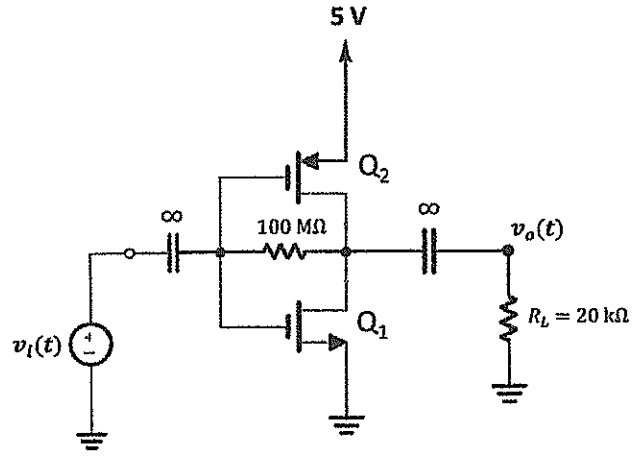

Fig. 3

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4. (a) Draw a cross section of the n-channel MOSFET operating in the saturation region. Label the terminals, channel, and doping type correctly in your plot. (5%)
(b) Following (a), please draw a high-frequency equivalent-circuit model. (5%)
(c) Re-draw (a) by adding the capacitances you used in (b) in your plot. (5%)
(d) Use (b) to derivate the unity-gain frequency f_T. (5%)

5. A CMOS inverter utilizes $V_{DD} = 5\,V, V_{tn} = |V_{tp}| = 1\,V$, and $\mu_n C_{ox} = 2\mu_p C_{ox} = 50\mu A/V^2$. Find $\left(\frac{W}{L}\right)_n$ and $\left(\frac{W}{L}\right)_p$ so that $V_M = 2.5$ V and so that for $v_I = V_{DD}$, the inverter can sink a current of 0.2 mA with the output voltage not exceeding 0.2 V. (10 %)

6. Figure 4 shows a CMOS SRAM memory cell. Consider the operation of writing a 1 into the cell that is originally storing a 0. Sketch the relevant part of the circuit and explain the operation. (10 %)

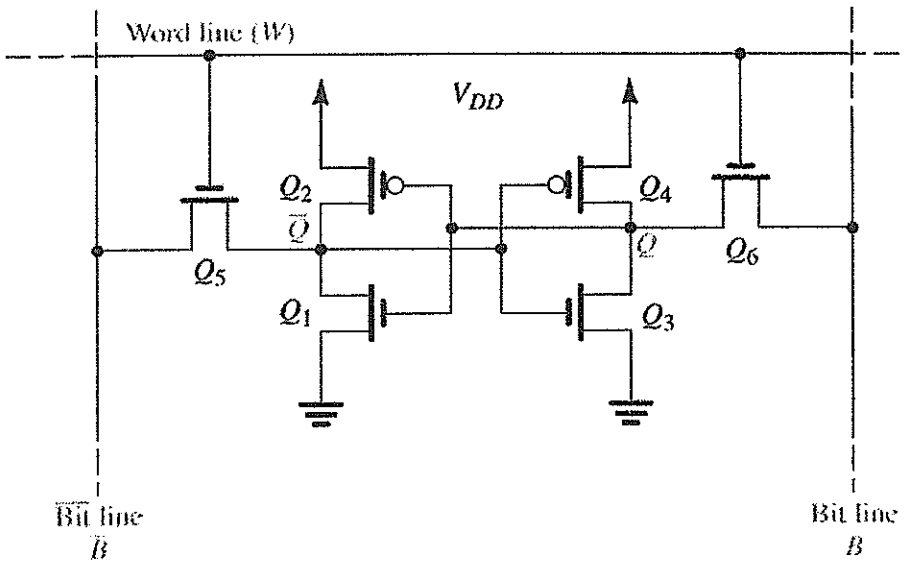

Fig. 4

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