1. (23%) Semiconductor physics

We know in semiconductors, atoms are orderly located in a "lattice" with a lattice constant ***a***. From the atomic point of view, each atom contributes a positively charged core that creates an energy potential for electrons. Assume for a single atom, electrons see a "potential function" like an infinite quantum well (Fig. 1-1) with the energy barrier (U) goes to infinity and the potential energy in the quantum well (0 < x < a) is zero. Let's see what happens next:

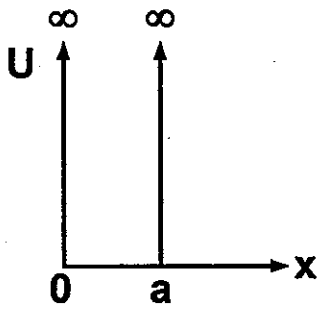

Fig. 1-1

(a) (3%) Write down the time-independent Schrödinger equation for an electron in the quantum well, the general solution, and the relationship between k and E, where k is the momentum and E is the energy of the electron.

(b) (8%) By normalization process, please solve the Schrödinger equation to get the wavefunctions and the associated energy levels for the first two subbands in the quantum well. **Show your calculation process to get your credits.**

(c) (3%) In reality, the atoms are located in a regular order (we call it a lattice) with a finite potential barrier (Fig. 1-2). Assume the subbands calculated from the infinite well in (b) can be still applied, and the first band (lower energy) represents the valence band and the second band (higher energy) represents the conduction band. Also assume the energy barrier becomes finite such that the wavefunctions are not "zero" at the boundary, instead penetrating into the barrier region. Please explain why those discrete subbands (dash lines in Fig. 1-2) will form continuous bands.

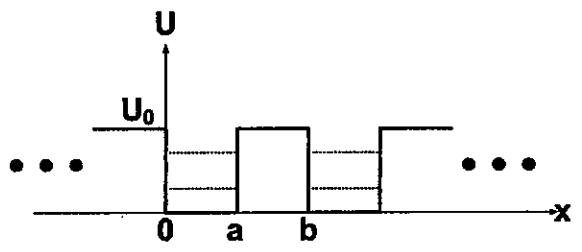

Fig. 1-2

(d) (3%) An electron travels with an initial velocity of zero ($v_i = 0$). In an electric field (E_{field}), it's accelerated to a final velocity v_f after a duration time of τ, and then collides (i.e. scattering event occurs) with the charged atomic cores and the velocity drops to zero. What's the mobility associated with the average velocity of the initial and final velocities? (Note: $v_f \neq v_{ave}$).

(e) (6%) Now assume the time between each collision is not the same, but with a specific probability distribution of a scattering probability of between time t and $t + dt$ being $e^{-\frac{t}{\tau}}\frac{dt}{\tau}$. Please calculate the average scattering duration by this probability distribution. Then show that the mobility is $\mu = e\tau/m$ by Newton's law.

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2. (12%) P/N junction

For a given square waveform as input signal, please draw the corresponding output waveforms for the following three circuits. Label all voltages.

(a) (2%) Draw output waveform of V_o for the circuit in Fig. 2-1 (b).

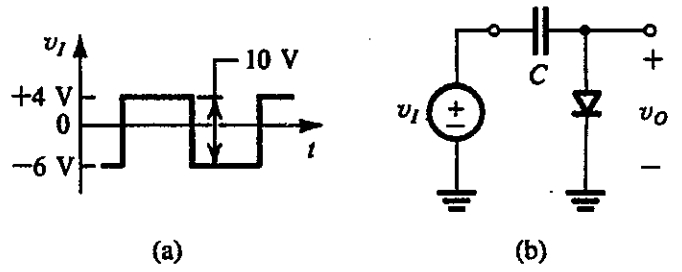

Fig. 2-1

(b) (4%) Draw waveforms of v_{D1} and V_o for the circuit (left) in Fig. 2-2.

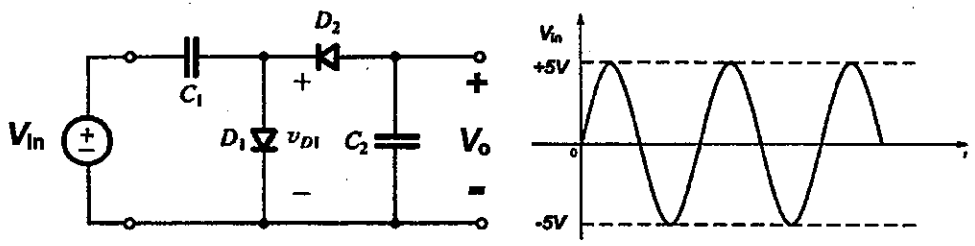

Fig. 2-2

(c) (6%) Draw waveforms of v_{D1} and V_o for the circuit (left) in Fig. 2-3.

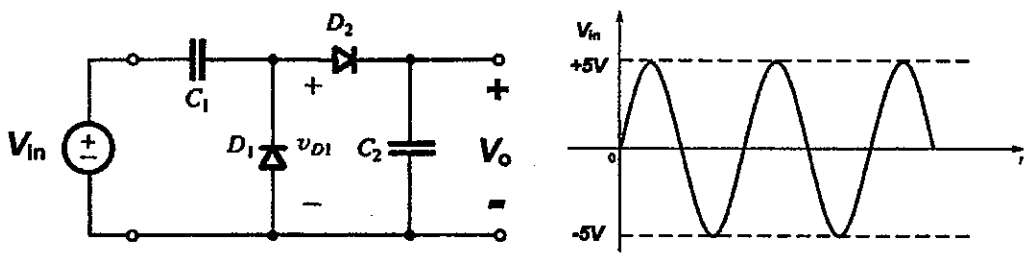

Fig. 2-3

3. (31%) MOSFET

Let's work out Moore's law, which states the transistor count (number of transistors) can be doubled every 18 or 24 months by the reduction of transistor dimensions. The current MOSFET structure is going from planar (Fig. 3-1 left) to Fin (Fig. 3-1 right). Apart from the better gate control offered by a Fin structure, a FinFET can also offer better performance.

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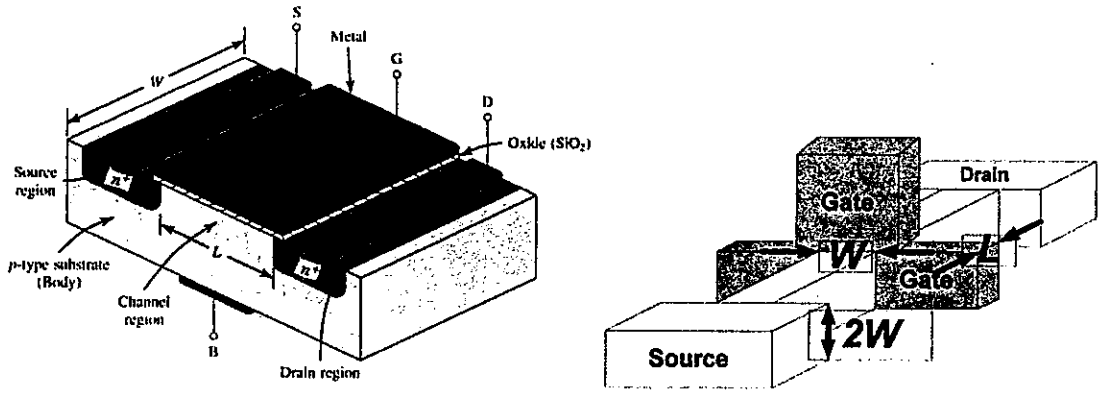

Fig. 3-1 (Left) A planar MOSFET; (Right) a FinFET

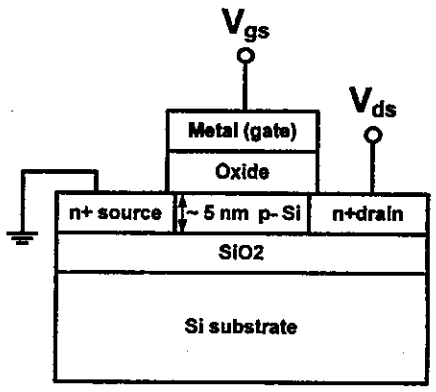

Fig. 3-2 An SOI Si MOSFET

(a) (2%) For a regular MOSFET, to increase the transistor count in a wafer without affecting the device performance (i.e. current level), we prefer to reduce the gate length. If the gate length is reduced by a factor of $\sqrt{2}$ **with the same current level,** <u>how many more transistors will you get on a wafer</u>? This gives you why the next generation of x nm node is always divided by $\sqrt{2}$ (e.g. 90 nm → 65 nm → 45 nm → 28 nm → 22 nm → 16 nm → 10 nm → 7 nm → 5 nm → 3 nm). Assume the wafe size is much larger than the transistor dimension.

(b) (6%) <u>Please draw the channel regions for FinFET structures in a cross sectional view of the fin</u>. <u>What's the enhancement factor of current by using a FinFET to replace a planar MOSFET</u>? **Note that the thickness of dielectric on top side of Fin is much larger than that on the sidewall, meaning that there won't be any inversion carriers at the top of the fin.** Also note that source and drain regions are right next to the gated region.

(c) (4%) However, to keep Moore's law alive, the reduction of the gate length leads to short-channel effects (SCEs) from the source to the drain either in the surface channel and in the bulk. To avoid that, one can use a FinFET. If we use a FinFET structure in Fig. 3-1 (right) to keep the same current level, we can keep the gate length at the level at which no SCE occurs. Let's say you now have a gate length of 20 nm and a width of 80 nm for a planar FET; for a FinFET, the gate length is 20 nm, the fin width is 10 nm, and the Fin height is 40 nm. <u>What is the ratio of transistor count on a wafer for FinFETs and planar MOSFETs</u>? Following the assumption in (b), **if we want to have the same current for each transistor**, by reducing the dimension of

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channel to 5 nm width, but keeping the same gate length, what is the ratio of transistor count if we increase the Fin height to 80 nm?

(d) (6%) Explain why you need a p-type substrate for a n-MOSFET. Note you have to answer why pn junctions between source/substrate and drain/substrate are required. Further, why can't we make a planar n-MOSFET on an n-type substrate with n^+source and n^+drain?

(e) (4%) For now, we have a new structure called "ultrathin-body silicon-on-insulator (UTBSOI)" MOSFET (Fig. 3-2). The channel doping is p-type and 10^{16} cm^{-3}. Please draw its depletion region and the channel region when the device is turned on.

(f) (9%) If we change the channel doping to n-type, unlike (d), it's still a transistor. Explain why. We usually call it a junctionless transistor. Is it n-MOSFET or p-MOSFET? Highlight its channel region when the device is ON. When the device is ON, is there any depletion region existing?

4. (34%) Feedback and Transistor Amplifiers

(a) (2%) See a linear network in Fig. 4-1. Given that $\frac{V_a}{V_b} = t$, show that $\frac{V_a}{V_c} = 1 - t$.

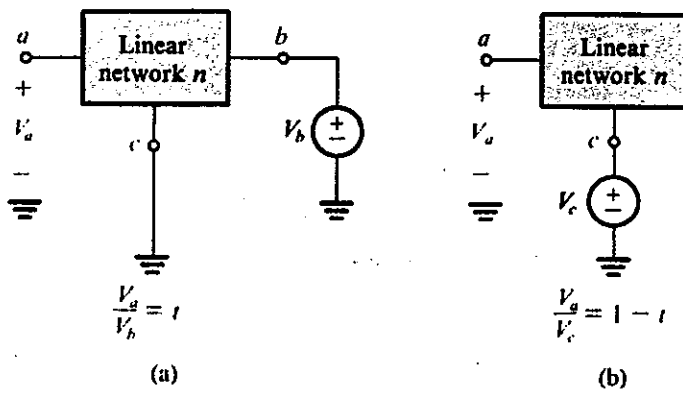

Fig. 4-1

(b) (6%) By the result in (a), please show that the two circuits in Fig. 4-2 are equivalent.

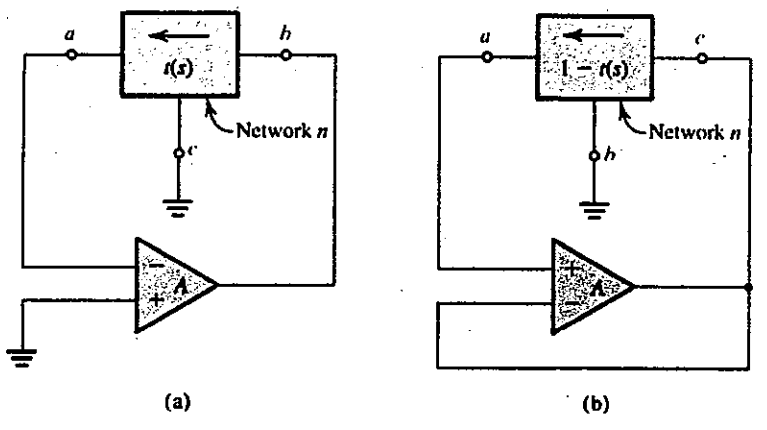

Fig. 4-2

(c) (4%) Consider a series-shunt feedback amplifier in Fig. 4-3. Please draw the feedback circuits consist of amplifier (A) and feedback parts (β).

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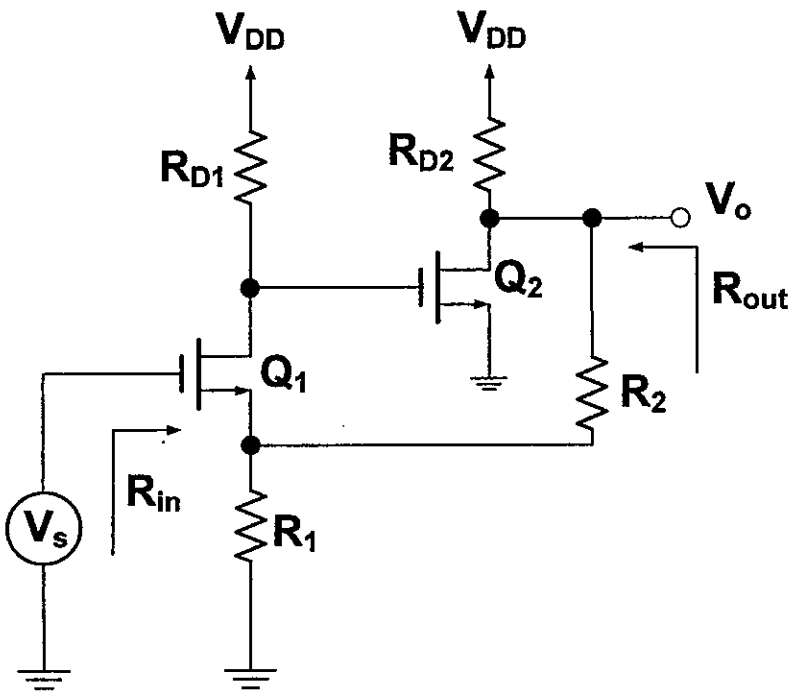

Fig. 4-3

(d) (15%) For the circuit in Fig. 4-3, if $g_{m1} = g_{m2} = 8$ mA/V, $R_{D1} = R_{D2} = 5$ kΩ, $R_1 = 1$ kΩ, and $R_2 = 9$ kΩ, by ignoring r_{o1} and r_{o2} of Q_1 and Q_2, respectively, please calculate (i) the voltage gain $\frac{V_0}{V_s}$, (ii) input resistance R_{in}, and (iii) output resistance R_{out}.

(e) (7%) For the circuit in Fig. 4-4, please draw its small signal circuit and derive the voltage gain $\frac{V_0}{V_{sig}}$.

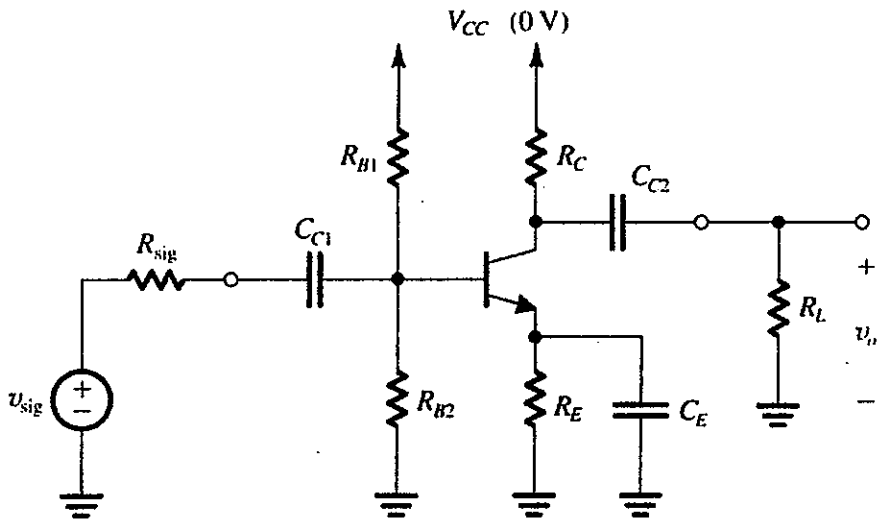

Fig. 4-4

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