※ 注意：請於試卷內之「非選擇題作答區」標明題號依序作答。

Please provide a full and clear explanation to EVERY question; otherwise, NO point is given.

1. (10%) We want to calculate two decimal numbers $(1.25)_{10} - (3.625)_{10}$ using 8-bit binary numbers. Please convert two numbers into binary and use two's complement to calculate the subtraction. Show your results in a binary number. Explain that your result is correct.
2. (15%) F is a function of three Boolean functions: X, Y, Z.

   $F(a,b,c,d) = G\,(X(a, b, c, d), Y(a, b, c), Z(b, c, d))$.

   Suppose $G = X \oplus Z + Y$. X is shown as a maxterm expansion $X = \Pi\, M(1, 2, 5, 7, 8, 10, 11, 13, 14, 15)$. $Y=(a'+b)(b+c)(a+c')$. $Z=bc'd+b'$. In this problem a is the most significant bit. That means, $abcd = 1000$ corresponds to minterm m_8.

   a) Please show the minterm expansion of $F(a, b, c, d)$. (5%)

   b) Perform the Shannon's Expansion of F with respect to input b. (5%)

   c) Please draw an implement of F using a two-to-one multiplexer with the select input b. Use 3-input PLA (programmable logic array) to implement the remaining logic functions for a, c, and d. Please minimize the number of product terms in PLA. (5%)
3. (20%) A sequence detector has two inputs XY and one output Z. The circuit examines groups of two consecutive inputs and produces an output $Z=1$ if the input sequence $\{X_1Y_1, X_2Y_2\} = \{00, 01\}$ or $\{10, 10\}$ occurs. X_1 means the first (left) X input and Y_1 means the first Y input. X_2 means the second (right) X input and Y_2 means the second Y input. The circuit resets after every two inputs $\{X_1Y_1, X_2Y_2\}$.

   a) Complete the following state graph in Fig. 3 for this sequence detector. Add new states if it is necessary. (5%)

   b) This is a Moore state machine. True or False? (5%)

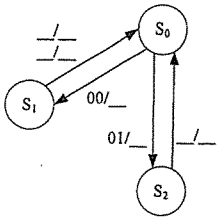

Fig. 3

   c) Write the state table for this detector. Design this detector using two T flip-flops (T=input and Q=output). Use straight assignments: $S_0=Q_1Q_2=00$, $S_1=Q_1Q_2=01$, $S_2=10$, and so on. Then $T_1 = Q_1+Q_2'X+Q_2Y$, True/False? $T_2=Q_2+Q_1'Y'$ True or False? (5%)

   d) We implement logic functions T_1 and T_2 using a ROM, please draw contents in the ROM. (5%)
4. (25%) For the sequential circuit in Fig. 4, which has one input X and one output Z.

   a) Write the next state equations. Write the output equation. (5%)

   b) Draw the state table and state graph of this circuit. Use straight assignments: $S_0=Q_1Q_2=00$, $S_1=Q_1Q_2=01$, $S_2=10$, $S_3=11$, where Q_1 is the output of FF1. (5%)

   c) Draw the timing chart for input sequence X = 10101. Suppose input X changes in midway between two falling clock edges. Assume initially $Q_1Q_2=00$. Mark false outputs of Z clearly in your timing chart, if any. (5%)

   d) Suppose the flip-flop propagation time (from clock edge to Q and Q') is 1.5ns. The flip-flop setup time is 1ns. The flip-flop hold time is 0.5ns. AND gate delay is 2ns. XOR gate delay is

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2ns. Suppose input X changes in midway between two falling clock edges. What is the minimum cycle time of this sequential circuit so that no setup-time violation will occur? (5%)

e) This circuit is guaranteed not to have hold-time violation regardless the arrival time of input X. True or False? (5%)

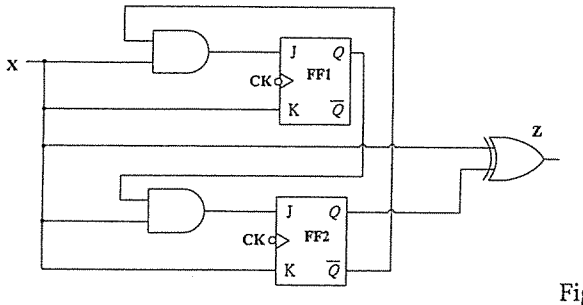

Fig. 4

5. (20%) Use Boolean algebra to answer the following questions. (Show all your work.)

a) Use consensus theorem to prove/disprove the following Boolean expression is correct. (5%)
$(a'+c'+d)(b+c'+d)(a+b+d)(a'+b+c)(a'+b+d)(a+b+c+d)(a+b+c+d') = (a'+c'+d)(b+d)(a+c)$

b) Use Boolean algebra to find the minimum three-level NOR gate circuit to implement $F=XY+XZ'W'+X'Y'Z$ (5%)

c) Factor out F to minimum product of sum. $F=A'C'D+AB'D'+CD'E+BD$
$= (A'+B+C+D')(A+B+C+D)(A+B+C'+D')(A'+B+D')(B+C'+D)(A+C+D)(B'+C+D)$ (5%)

d) For the function F in problem **c)**, how many different input assignments are there such that F=0? (5%)

6. (10%) A sequential circuit has one input X and two outputs (YZ). YZ represents a 2-bit binary number equal to the total number of pairs of adjacent 1's in X that has been received. The circuit resets after total pairs of 1's reaches four. The following sequence shows an example. Pease note that, after reset, the state machine forgets the previous overlapping 1's (as underlined). Design a Moore state graph for this circuit using minimum number of states. S_0 represents the reset state.

X	0	1	0	1	1	0	1	1	1	0	0	1	0	1	1	1	0	1	1	1	…
Y	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	1	…
Z	0	0	0	0	1	1	1	0	1	1	1	1	1	1	0	0	0	0	1	0	…

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