420 國立臺灣大學 103 學年度碩士班招生考試試題

: 電子學(C)

題號: 420

頁之第 頁

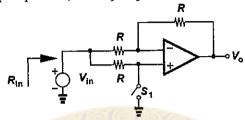
節次: 8

※ 注意:請於試卷上「非選擇題作答區」內依序作答,並應註明作答之大題及其題號。

共四大題

Problem 1: (30 pts, 3 pts each, 填充, 中英皆可)

(a) For the following op amp circuit, if the op amp is ideal



(1) When switch S_1 is ON, what is the close-loop gain $(V_o/V_{in}) = ($) and

(2) When switch S_1 is OFF, what is the close-loop gain $(V_0/V_{in}) = ($) and

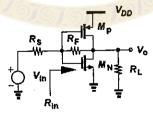
 $R_{\rm in} = ($

(

(b) For a CMOS current mirror as follows, what are TWO factors to induce the current mismatch between M_1 and M_0 ? The nominal size for M_1 and M_0 are the same.



(c) For the following circuits, please neglect channel length modulation and derive the following parameters by g_{mp} , g_{mn} , R_F and R_L . Note that g_{mp} and g_{mn} are the transconductance for M_P and M_N , respectively.



(1) $R_{\rm in} = ($

(2) close-loop gain $(V_0/V_{in}) = ($

(d) For a real op amp, it has the following nonideal effect, (I) finite open-loop gain, (II) finite output impedance, (III) finite max/min output swing, (IV) finite slew rate and (V) finite small-signal bandwidth. Please use (I), (II) and so on for the answers.

見背面

題號: 420

國立臺灣大學 103 學年度碩士班招生考試試題

科目:電子學(C)

節次: 8

共 马 頁之第 2 頁

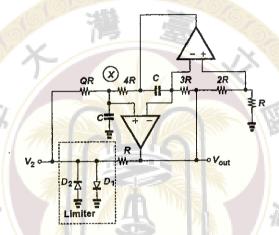
(1) Which ones can induce linear error (no harmonic distortion at the output)?

(9)

(2) Which ones can induce non-linear error (with harmonic distortion at the output)?

Problem 2~4 計算題,請寫過程

2. (28pts) The active-filter tuned oscillator is shown as below. If C is equal to 1 nF and R is equal to 1.6 K Ω . Note that Q is quite large.



- (a) (5 pts) What is the oscillation frequency?
- (b) (6pts) If the turn-on voltage of the diode is 1V, what is the peak-to-peak amplitude at node X? No score will be given without derivation. Is it a sine wave or square wave? (Hint: A square wave with peak-to-peak amplitude of V volts has a fundamental component with $4V/\pi$ volts peak-to-peak amplitude).
- (c) (5 pts) If we move the limiter to node X, what is the peak-to-peak amplitude at the output V_{out} ?
- (d) (12 pts) Now, the op amp has parasitic input capacitance 0.1 nF at both positive and negative input nodes. Please repeat part (a)
- 3. (25 pts) For the following circuit in Fig. 3-1, neglect body effect in all transistors. Note that $(W/L)_{1,2}$ =40/1, $(W/L)_{3,4}$ =100/1, $\mu_n C_{ox}$ =50 μ A/V², $\mu_p C_{ox}$ =20 μ A/V², V_{An} =100 V, $|V_{Ap}|$ = 66.67 V, V_{tn} =0.5 V, and V_{tp} =-0.5 V.

接次頁

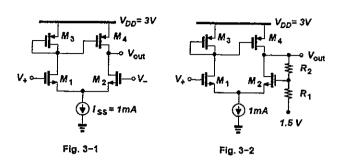
題號: 420 國立臺灣大學 103 學年度碩士班招生考試試題

科目:電子學(C)

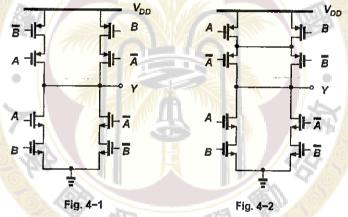
節次: 8

題號: 420

共 马 頁之第 う 頁



- (a) (10 pts) First, let's set $V_+ = 1.5 \text{ V} + 0.001 \sin(\omega t)$ and $V_- = 1.5 \text{ V}$. What is V_{out} ? Please include both DC and AC.
- (b) (15 pts) Now, a resistive feedback network is included as shown in Fig. 3-2, where $R_2=100$ K Ω and $R_1=10$ K Ω . What is V_{out} if $V_+=1.5$ V+ 0.001 $\sin(\omega t)$?
- 4. (17 pts) In this problem, we want to study CMOS logic gate design,



(a) (7 pts) Shown in the following Fig. 4-1 and Fig. 4-2, explain why these two designs can generate identical logic function? What is Boolean function? Which topology would you prefer in practical design? Explain why you choose such topology. Note that $A, \overline{A}, B, \text{ and } \overline{B}$ are the logic inputs and Y is the output.

Now, use Fig Fig. 4-1 for the following questions,

- (b) (4 pts) Choose proper PMOS/NMOS size ratio to obtain identical worst-case the propagation delay of high to low (T_{phl}) and low to high (T_{plh}). Please identify the worst-case H-> L and L->H condition.
- (c) (6 pts) By using the size in (b), if we choose $V_{dd}=3V$ and $V_{tn}=|V_{tp}|=0.5V$, what is the switching threshold voltage V_m ? Note that V_m is defined as an input voltage, V_{in} , would generate an output voltage that is the same as the input voltage. Note that $V_B=3V$ and $V_A=V_{in}$. Body effect should be neglected for simplicity.

試題隨卷繳回