※ 注意：請於試卷上「非選擇題作答區」內依序作答，並應註明作答之大題及其題號

第一部分為選擇題，答案可能不只一個，需全對才給分。共 10 題，每題 5 分。

1. Please select the correct one(s) about the characteristics of the ideal Op amp.
   (A) Infinite input impedance
   (B) Infinite output impedance
   (C) Infinite common-mode gain
   (D) Infinite closed-loop gain
   (E) Infinite bandwidth

2. Please select the correct one(s) about the characteristics of a real silicon diode.
   (A) As temperature increases, the voltage required to maintain a constant current will also increase.
   (B) As temperature increases, the saturation current will also increase.
   (C) A diode in reverse biased can be used for voltage regulation.
   (D) A diode in reverse biased will not conduct any current.
   (E) The larger the size, the higher the saturation current.

3. Please select the correct one(s) about the characteristics of an *npn* silicon BJT.
   (A) The current is mainly composed of electron drift current under base-emitter junction forward bias.
   (B) The current gain β in active mode operation is smaller than the β in saturation mode operation.
   (C) The common-base configuration has better high-frequency response than the common-emitter one.
   (D) If we consider Early effect, the small-signal gain will decrease.
   (E) Breakdown voltage BV_{CBO} is usually half BV_{CEO}

4. Please select the correct one(s) about the characteristics of a silicon NMOS.
   (A) The current is mainly composed of electron drift current under drain-source terminal forward bias.
   (B) Increasing oxide thickness will cause the transconductance g_m to decrease.
   (C) The Body effect will reduce threshold voltage and increase drain current.
   (D) Including a resistor in the source lead of the common source stage can effectively increase gain.
   (E) In general, an NMOS provides more gain compared to an *npn* BJT when applying in the amplifier design.

5. Please select the correct one(s) about the characteristics of different types of amplifiers.
   (A) We stack a common-emitter transistor on top of a common-base transistor to raise the output resistance.
   (B) A MOS cascode amplifier with a cascode current-source load achieves a gain of $(g_m r_o)^2$.
   (C) The Widlar current source provides a way to implement a low-valued constant-current source that also has a high output resistance.
   (D) In the MOS differential pair amplifier, to steer the current completely to one side of the pair, a difference input voltage of $2V_{OV}$ is needed.
   (E) Differential amplifiers do not need bypass and coupling capacitors.

6. Consider a 10-output current mirror in Fig. 1. Assume that all transistor are matched and have finite $\beta = 100$ and ignoring the effect of finite output resistances. If $I_{REF} = 10$ mA. What is the value of I_{10}?
   (A) 7 mA (B) 8 mA (C) 9 mA (D) 10 mA (E) 11 mA

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7. Consider a CC-CE amplifier in Fig. 2. Assume $I_1 = I_2 = 1$ mA, Q_1 and Q_2 are matched. $\beta = 100$, $C_\pi = 13.9$ pF. $C_\mu = 2$ pF. Let the amplifier be fed with a source V_{sig} with $R_{sig} = 4$ KΩ, and load resistance $R_L = 4$ KΩ. Which *RC* delay term(s) may have more significant impacts on the determination of 3-dB frequency f_H?
(A) $C_{\mu 1}R_{\mu 1}$ (B) $C_{\mu 2}R_{\mu 2}$ (C) $C_{\pi 1}R_{\pi 1}$ (D) $C_{\pi 2}R_{\pi 2}$ (E) $C_{\pi 1}R_{\mu 2}$

8. Please select the correct one(s) about the characteristics of a CMOS logic inverter.
(A) The basic building block of digital circuits.
(B) The static power dissipation is the result of current flow in either 0 or 1 state or both.
(C) The maximum frequency at which an inverter can be switched is related to its propagation delay by $f_{max} = 1/\sqrt{2}t_p$.
(D) Larger W/L ratios can result in a reduction in t_p.
(E) Pull-down network (PDN) comprises PMOS transistors.

9. Please select the correct one(s) about the properties of feedback amplifiers.
(A) To build a oscillator, we need to have a positive feedback network with $A\beta \geq 1$.
(B) The shunt-series feedback topology is best suited for voltage amplifiers.
(C) For the feedback amplifier to be stable, most of its poles must be in the left half of the *s* plane.
(D) A smaller pole Q factor will have a more flat and larger gain response.
(E) At frequency ω_{180}, unstable amplifiers have the magnitude of the loop gain greater than one.

10. Consider the CMOS realization of a logic gate in Fig. 3. What is the output *Y*?
(A) $\overline{A + B(C + D)}$ (B) $\overline{A + BCD}$ (C) $A(B + CD)$ (D) $\bar{A} + \overline{B + CD}$ (E) $A + \overline{(B + CD)}$

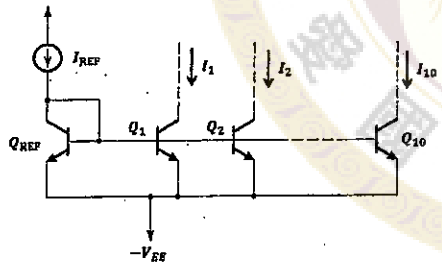

Fig. 1

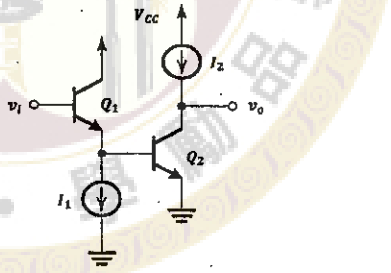

Fig. 2

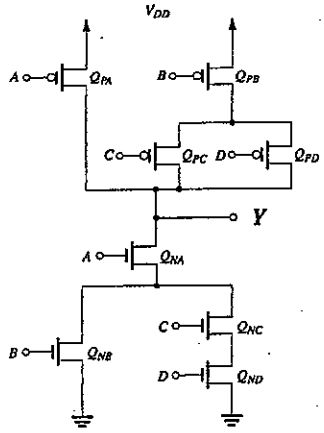

Fig. 3

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第二部分為簡答題，視答對程度部分給分。

11. Draw the time-dependent output waveforms of v_o, v_+, v_- in Fig. 4. Label correctly the corresponding periods, magnitudes, time constants in your plot using $T_1, T_2, L_+, L_-, R_1, R_2, R_3, C$. (10%)

12. For the circuit in Fig. 5. Assume all the transistors, including those that implement the current sources, are operating at equal overdrive voltages of 0.3 V magnitude and have $|V_t| = 0.7\,V$. In order to operate properly, each of the current sources requires a minimum voltage of $|V_{OV}|$ across its terminals. What is the range over which **both** NMOS and PMOS input stages operate? (10%)

13. The circuit in Fig. 6 is considered an amplifier. Assume that $K_n=k_p$= 400 μA/V^2, $V_{tn}=|V_{tp}|$=1V, R_s= 2.5 kΩ, R_L=20 kΩ and R_G=100 MΩ.
    (a) What is the dc current of the NMOS transistor? (5%)
    (b) If $v_i(t) = 0.05\sin(300t)$V, find the output voltage $v_O(t)$. (10%)

14. Consider the CMOS op amp circuit in Fig. 7. $\mu_n C_{ox} = 3\mu_p C_{ox} = 90\ \mu A/V^2$, $|V_t|$=0.7 V, and $V_{DD}=V_{SS}$=2.5 V. For a particular design $I = 100\,\mu A$, $(W/L)_1 = (W/L)_2 = (W/L)_5 = 200$, and $(W/L)_3 = (W/L)_4 = 100$
    (a) What is the transistor sizing constraint to eliminate dc offset? (5%)
    (b) Find the (W/L) ratios of Q_6 and Q_7 so that $I_6 = 100\mu A$ (5%)
    (c) Find g_m for Q_1 and Q_6 (5%)

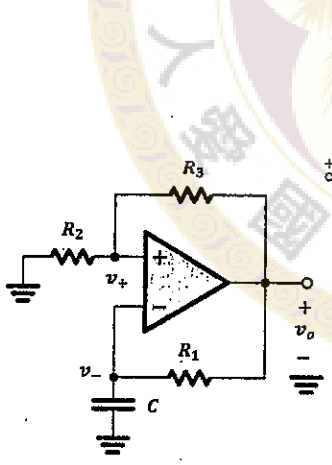

Fig. 4

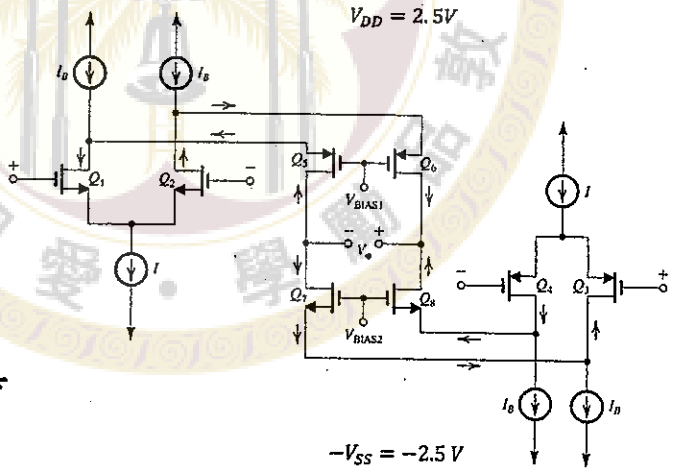

Fig. 5

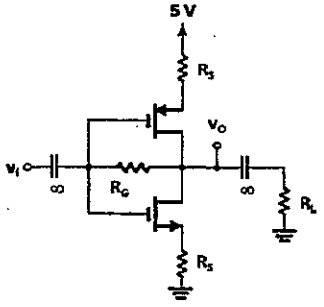

Fig. 6

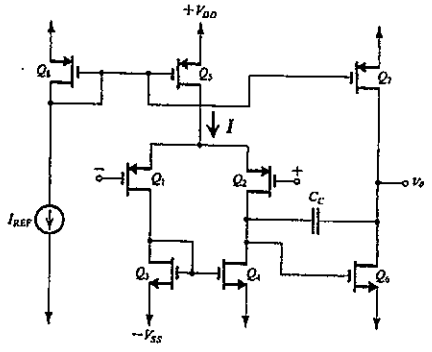

Fig. 7

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