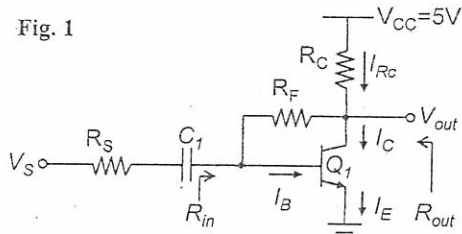第一大題為選擇題(複選)，共 25 小題，每小題 2 分，請作答於『答案卡』中。第二、三、四大題為計算題，請於試卷上作答。

一、選擇題(複選) (50%)

Fig. 1

For questions 1 to 5, please refer to Fig. 1.

For the BJT, Q_1, in Fig. 1, assume $\beta=100$ and $v_{BE}=0.7V$. Let the thermal voltage $V_T=25mV$, $R_C=2k\Omega$, $R_F=100k\Omega$, and $R_S=1k\Omega$. C_1 is a coupling capacitor. Ignore the Early effect.

1. Perform DC analysis and find out which of the following(s) is (are) true. (A) $I_B \approx 14.2\mu A$. (B) Collector voltage of $Q_1 \approx 2.1V$. (C) $I_{Rc} \approx 1.434mA$. (D) $I_{Rc} = I_C$.

2. What kind of feedback topology is used in this circuit? (A) Shunt-shunt. (B) Series-shunt. (C) Shunt-series. (D) Series-series.

3. Which of the following(s) is (are) true? (A) $g_m = I_C/V_T$. (B) $r_e = \alpha/g_m$. (C) $r_e = V_T/I_E$. (D) $\beta = g_m \times r_\pi$.

4. Regarding R_{in}, which of the following(s) is (are) true? (A) $R_{in} = [r_\pi \times (R_F+R_C)]/[r_\pi+R_F+(\beta+1)\times R_C]$. (B) $R_{in} = r_\pi||(R_F+R_C)$. (C) If $R_F \to \infty$, R_{in} is infinite. (D) If $R_F \to 0$, $R_{in} = r_\pi||(1/g_m)||R_C$.

5. Regarding G_V ($\equiv V_{out}/V_S$), which of the following(s) is (are) true? (A) $G_V \approx -g_m \times R_C$ (B) $G_V \approx -\beta \times R_C/(r_\pi+R_S)$. (C) $-g_m \times R_C \times [R_{in}/(R_{in}+R_S)]$ (D) $G_V \approx -113.6$. (E) $G_V \approx -72.4$.
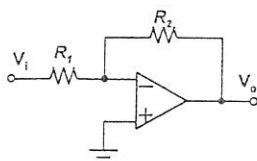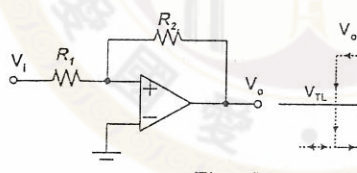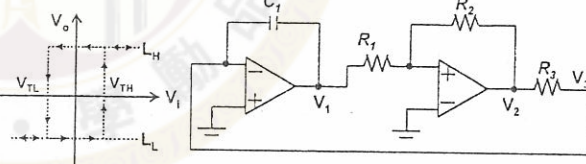

Fig. 2(a)　　　Fig. 2(b)　　　Fig. 2(c)

For questions 6 to 10, please refer to Fig. 2(a) ~ 2(c). Assuming all operational amplifiers are ideal.

6. For the circuit shown in Fig. 2(a), which of the following(s) is (are) true? (A) It is an inverting amplifier. (B) It is a non-inverting amplifier. (C) $V_o/V_i = -R_2/R_1$. (D) $V_o/V_i = 1+(R_2/R_1)$.

7. For the circuit shown in Fig. 2(b), which of the following(s) is (are) true? (A) It is an astable circuit. (B) It has an inverting transfer characteristic. (C) It is a Schmitt trigger. (D) It can be used as a memory element.

8. The right plot of Fig. 2(b) shows the voltage transfer curve for the circuit shown in the left of Fig. 2(b), where L_H and L_L are the output voltages when the circuit is saturated. Find V_{TH} and V_{TL}. (A) $V_{TH} = -L_L \times (R_1/R_2)$. (B) $V_{TL} = -L_H \times (R_1/R_2)$. (C) $V_{TH} = L_H \times (R_1/R_2)$. (D) $V_{TL} = L_L \times (R_1/R_2)$.

9. For the circuit in Fig. 2(c), which of the following(s) is (are) true? (A) V_1 is a square wave. (B) V_2 is a square wave. (C) V_3 is a square wave. (D) V_1 is a tri-angular wave.

10. Let $L_H = -L_L$, find the period (T) for the signals generated by the circuit shown in Fig. 2(c). (A) $T = 0.5 \times R_3 C_1 (V_{TH}-V_{TL})/L_H$. (B) $T = R_3 C_1 (V_{TH}-V_{TL})/L_H$. (C) $T = R_1 C_1 (V_{TH}-V_{TL})/L_H$. (D) $T = 2 \times R_3 C_1 (V_{TH}-V_{TL})/L_H$.

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Fig. 3(a)　　Fig. 3(b)　　Fig. 3(c)　　Fig. 3(d)　　Fig. 3(e)
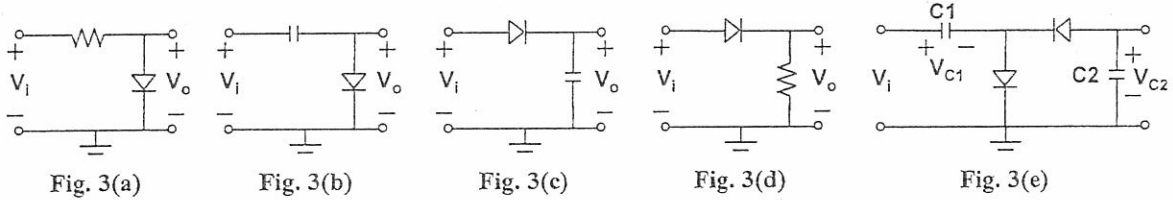
For questions 11 to 15, please refer to Fig. 3(a) ~ 3(e).

11. What is the function of the circuit in Fig. 3(a)? (A) A rectifier. (B) A limiting circuit. (C) A DC restorer. (D) A peak detector.

12. What is the function of the circuit in Fig. 3(b)? (A) A rectifier. (B) A limiting circuit. (C) A DC restorer. (D) A peak detector.

13. What is the function of the circuit in Fig. 3(c)? (A) A rectifier. (B) A limiting circuit. (C) A DC restorer. (D) A peak detector.

14. What is the function of the circuit in Fig. 3(d)? (A) A rectifier. (B) A limiting circuit. (C) A DC restorer. (D) A peak detector.

15. For the circuit shown in Fig. 3(e), assuming the diodes are ideal and $V_i = V_P \times \sin(\omega t)$, which of the following(s) is (are) true? (A) $V_{C1} = V_P$. (B) $V_{C1} = -V_P$. (C) $V_{C2} = V_P$. (D) $V_{C2} = 2V_P$. (E) $V_{C2} = -2V_P$.

Fig. 4(a)　　　Fig. 4(b)　　　Fig. 4(c)
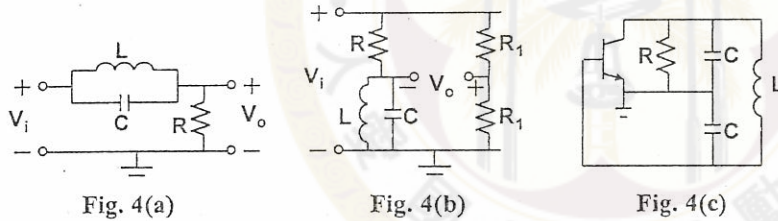
For questions 16 to 18, please refer to Fig. 4(a) ~ 4(c).

16. For the circuit shown in Fig. 4(a), what kind of filter function does it realize? (A) Low-pass. (B) High-pass. (C) Band-pass. (D) Notch. (E) All-pass.

17. For the circuit shown in Fig. 4(b), what kind of filter function does it realize? (A) Low-pass. (B) High-pass. (C) Band-pass. (D) Notch. (E) All-pass.

18. For the circuit shown in Fig. 4(c), which of the following(s) is (are) true? (A) This is a Colpitts oscillator. (B) This is a Hartley oscillator. (C) Additional limiting circuit is required to stabilize the oscillation amplitude. (D) The resonant frequency, $\omega_0 = 1/\sqrt{LC}$. (E) $\omega_0 = 1/\sqrt{LC/2}$.

19. Which of the following(s) regarding the SRAM is (are) true? (A) The read operation is destructive. (B) SRAM is volatile. (C) SRAM uses latch to store data. (D) SRAM needs to be refreshed.

20. Which of the following(s) regarding the DRAM is (are) true? (A) The read operation is destructive. (B) DRAM is volatile. (C) DRAM uses capacitor to store data. (D) DRAM needs to be refreshed.

21. Which of the following(s) regarding the "CMOS logic circuit" is (are) true? (A) It does not consume static current. (B) NAND gates are generally preferred over NOR gates for implementing combinational logic functions. (C) Pull-up network (PUN) and pull-down network (PDN) can be designed as dual networks. (D) PUN is implemented using NMOS transistors.

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22. Which of the following(s) regarding the "pseudo-NMOS logic circuit" is (are) true? (A) It does not consume static current. (B) It is a ratioless design. (C) t_{PHL} is always larger than t_{PLH}. (D) Compared with the CMOS logic circuit, the pseudo-NMOS logic circuit use less transistors when implementing the same logic function.

23. Which of the following(s) regarding the "pass-transistor logic circuit" is (are) true? (A) It does not consume static current. (B) The NMOS switch can deliver a "good 0". (C) The PMOS switch can deliver a "good 1". (D) The PMOS switch can deliver a "good 0".

24. Which of the following(s) regarding the "dynamic logic circuit" is (are) true? (A) It does not consume static current. (B) It needs to be periodically refreshed. (C) It is a ratioless design. (D) It suffers from charge sharing phenomenon.

25. Which of the following(s) regarding digital logic circuits is (are) true? (A) Increasing power supply voltage can always reduce circuit delay. (B) Increasing the ratio of W/L can always reduce circuit delay. (C) Reducing the circuit operation frequency can always reduce power consumption. (D) A larger trans-conductance parameter ($k'=\mu \times C_{OX}$) can always result in a shorter circuit delay.

第二、三、四大題為計算題，請於試卷上作答。

二、The operational amplifier (Op Amp) is one of the most important circuit blocks used in various applications. To implement the operational amplifier, both MOSFET and BJT can be used to achieve the desired performance. Please answer the following questions.

(a) Please list the five fundamental characteristics of ideal Op Amps. (5%)

(b) To achieve the ideal characteristics listed above, it typically uses three cascade stages to design an Op Amp. Please use CC, CB, and CE (the three single-stage BJT amplifier configurations) as examples to realize each stage and briefly explain why you want to use them. (Hint: In general, the combination of different configurations is needed within one stage, such as CE-CC.) (9%)

(c) In general, all the Op Amps have imperfections. To conquer these imperfections, we have to carefully choose the transistor, MOSFET or BJT, depending on the required performance. (10%)

(1) Without temperature compensation circuit, which kind of transistor will you use to obtain the thermal stability? Justify your answer.

(2) To minimize the input bias current, which kind of transistor will you use? Justify your answer.

(3) To have better frequency bandwidth, which kind of transistor will you use? Justify your answer.

(4) To have better current-handling capability, which kind of transistor will you use? Justify your answer.

(5) To have advantages from both kinds of transistors, BiCMOS process has been developed. Please explain what BiCMOS is and its major advantage.

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三、This question is referred to Fig. 5. (16%)

(a) Design a circuit such that I_{D1}=0.2mA, I_{D2}=0.5mA, V_{DS1}=2V, and V_{SD2}=3V.

(b) Determine the small-signal voltage gain A_v=v_O/v_i. The transistor parameters are V_{TN1}=0.6V, V_{TP2}=-0.6V, K_{n1}=0.2mA/V^2, K_{p2}=1.0mA/V^2, and λ_1=λ_2=0. In addition, V_{DD}=5V, and R_{in}=400k.
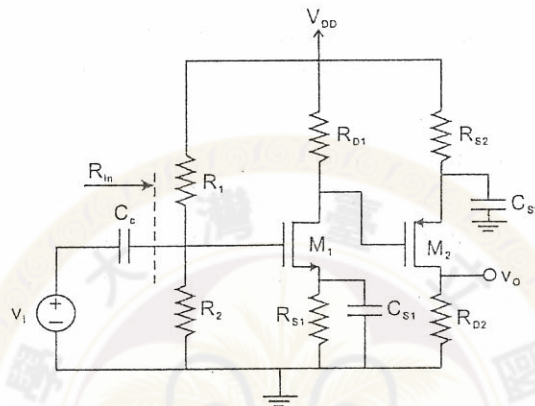

Fig. 5

四、This question is referred to Fig. 6. (10%)

(a) Draw the simplified high-frequency equivalent circuit.

(b) Calculate the equivalent Miller capacitance. The transistor parameters are K_n=1mA/V^2, V_{TN}=2V, λ=0, C_{gs}=50fF, and C_{gd}=8fF.

Fig. 6

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