*請依題號順序作答

一、簡答題(可以使用圖示輔助說明) (25%)

1. Name two reasons why a current mirror load is used in differential amplifiers. (4%)
2. To design an op-amp, you can use bipolar transistor or CMOS technologies. Which technology would you choose to use and why? Provide at least three main reasons you can think of. (6%)
3. What is the channel modulation effect in MOS transistor? Please explain it and also describe it effects on the MOS transistor behaviors (4%)
4. Name two advantages of using emitter degeneration in an emitter-coupled differential pair and explain it. (4%)
5. Please list the current components within the biopolar transistor under the active mode. In addition, please also draw the minority-carrier concentration in the biopolar transistor. (7%)

二、計算題 (75%)

1. (20%) The current source shown in Figure 1 uses both bipolar and MOS technology. Calculate I_0 by the parameters given below. Please also derive the equation for R_O.
   Bipolar Data: $\beta = 100$; $V_A = 50V$; $r_\mu = \infty$
   MOS Data: $\mu_n C_{ox} = 50\mu A/V^2$; $V_{t0} = -0.5V$; $\lambda = 0.02V^{-1}$; $W/L = 20/1$; Negelect body effect

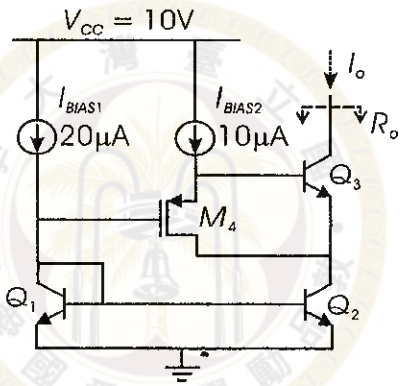

Figure 1

2. (15%) For the amplifier circuit shown in Figure 2, please determine equations and numerical values for the indeicated parameters: (a) v_O/v_S; (b) bandwidth f_H.
   NMOS Data: $\mu_n C_{ox} = 60\ \mu A/V^2$; $V_{t0} = 0.7V$; $\gamma = 0.5V^{1/2}$; $C_{gs1} = 150fF$; $C_{gd1} = 20\ fF$; $C_{sb1} = 50fF$; $C_{db1} = 70fF$; $2\phi_f = 0.6V$; $W/L = 100/1$
   Bipolar Data: $\beta_2 = 100$; $V_{A2} = 200V$; $C_{\mu 2} = 50fF$; $f_{T2} = 10GHz$

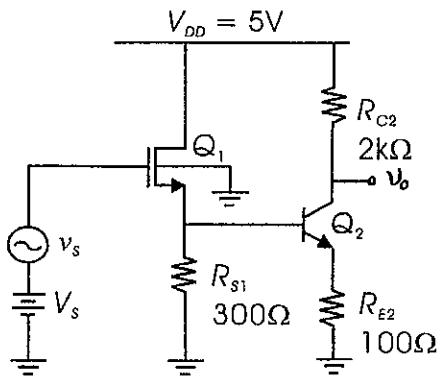

Figure 2

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3. (40%) This is the integrated circuit operational amplifier circuit, shown as Figure 3. The data for the biopolar devices and the bias points can be shown as follows. Please answer the following questions.
(a) In the input stage, which one is the non-inverting input terminal, A or B? (2%)
(b) List three advantages of the input stage in this design. (6%)
(c) Determine the values of R_1 and R_2 so that I_{C12} = 1mA and I_{C7} = 50 μA. For this part, you can neglect the base current. (6%)
(d) Assume the bias circuit has been designed to obtain the intended bias point, i.e. assume R_{E9} is designed so that I_{C9} = 40μA). With the base of Q2 grounded, derive the first stage gain (V_C/V_A) and calculate its value. In addition, derive the values for the relevant collector currents. (10%)
(e) Derive the second stage gain (V_D/V_C) and calculate its value. Assume a positive output voltage and write down the values for the relevant collector currents. (10%)
(f) Derive an expression and calculate the numerical value for the common-mode rejection ratio (CMRR) of this op amp. (6%)

Bipolar Device Data: for npn: β_n = 100, V_{AN} = 200V; for pnp: β_p = 50; V_{AP} = 50V
For small signal analysis: C_μ = 3pF; C_{CS} = 6pF; C_π = 20pF; $V_{BE(on)}$ = 0.7V; $V_{CE(sat)}$ = 0.2V
Intended Biasing: $I_{C7} = I_{C8}$ = 50μA; I_{C9} = 40μA; I_{C12} = 1mA

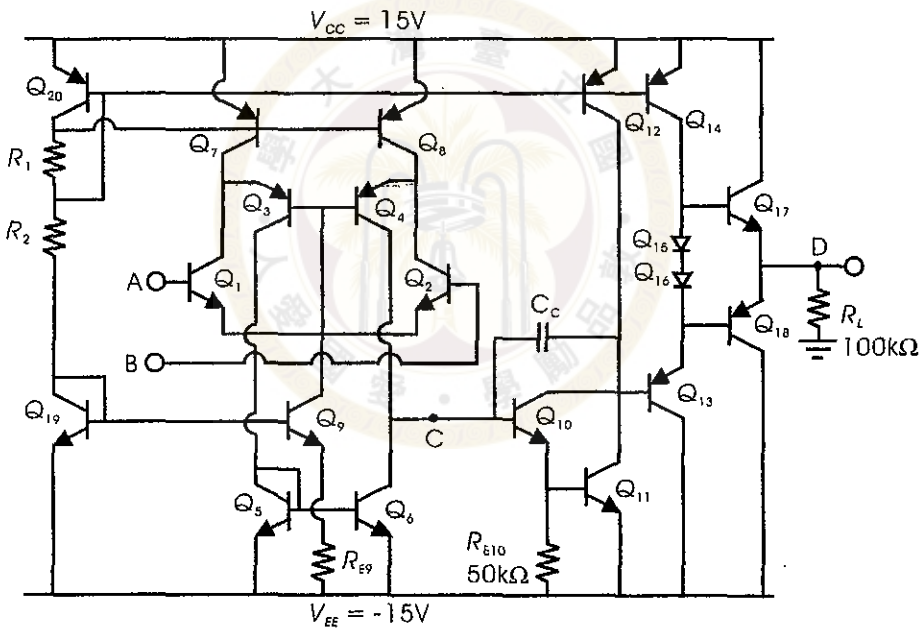

Figure 3

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