第一部份：填空題 (15 pt)
1. **Memory (row-address decoder): (6 pt)**
   (a) (4 pt)
   Assume there are 5 bits in the row addresses, there are \( (A) \) word lines. By using NOR gate array with Boolean operation such as \( W_i = A_0 \cdot \cdots \cdot A_j \) (Fig. 1(a)), you will need \( (B) \) NMOS transistors to implement this decoder. Note: the figure shows the 3-bit NOR decoder structure. Make the analogy for 5-bit case.

   (b) (2 pt)
   If now you’d like to reduce the transistor counts, you can use a tree structure (Fig. 1(b)) to cut down the number to \( (C) \).

   ![Fig. 1 (a)](image1)
   ![Fig. 1 (b)](image2)

2. **BJT Basics: (6 pt)**
   (a) (2 pt)
   There are two bias conditions: forward and reverse biases. For a BJT (n-p-n) device to be an amplifier (operated in the active region), you need a \( (D) \) biased base/emitter junction and a \( (F) \) biased base/collector junction.

   (b) (2 pt)
   There are two type of carriers: electrons and holes. The carriers representing output signals (collector current, \( I_C \)) in an n-p-n BJT are \( (F) \). The carriers representing input signals (base current \( I_B \)) in an n-p-n BJT are \( (G) \).

   (c) (2 pt)
   There are two mechanisms for carrier transport: drift and diffusion. The current in a BJT is dominated by \( (H) \). The current in a MOSFET is dominated by \( (I) \).

3. **OP AMP: (3 pt)**
   (a) (1 pt)
   For an open-loop OP AMP circuit, when you have an input voltage difference \( V_{in} = V_s - V_r \) with a gain \( A \) of OP AMP, you will get output \( V_{out} = \) ________________.
(b) (2 pt)

For a closed-loop OP AMP circuit, you usually assume the voltages at negative and positive terminals of OP AMP are the same. If so, $V_{in} = V_+ - V_- = 0$ and $V_{out} = A(V_+ - V_-)$ will be 0, too. Right or wrong? (No need to explain).

4. Oscillator/Filter: (16 pt)

(a) (12 pt)

Please derive the feedback network gain $\beta = \frac{V_+}{V_{out}}$ (which is enclosed in the dash rectangles) for the circuits in Fig. 4 (a) and (b)

![Fig. 4 (a)](image)

![Fig. 4 (b)](image)

(b) (4 pt)

Which circuit will oscillate and what is the oscillation frequency $\omega$?

5. MOSFETs (40 pt)

A common source amplifier is plotted in Fig. 5-1 (a) with its VTC shown in Fig. 5-1 (b). The DC bias parameters: $V_{DD} = 1.8$ V, $R_D = 17.5$ kΩ, $V_{th} = 0.4$ V, $k_n = 4$ mA/V$^2$, and ignore the channel length modulation effect.

![Fig. 5-1](image)

(a) (8 pt)

Determine the values of $V_{GS}$ and $V_{DS}$ at point A and B in Fig. 5-1 (b). Hint: for point A, NMOS is just turned on ($V_{GS} = V_{th}$). For point B, the NMOS is operated at the boundary of the saturation and triode modes.
(b) (12 pt)
What are current values \( I_D \) at point A and B? What are \( g_m \) values at point A and B? What are voltage gain \( A_v \) (\( = \frac{V_{DS}}{V_{GS}} \)) at point A and B?

(c) (4 pt)
What are noise margins for low \((NM_L)\) and high inputs \((NM_H)\)? (Hint: you don’t need to calculate the exact values of \( V_{IL} \) and \( V_{IH} \) at slope = -1, but approximately use \( V_{OL} \approx 0, V_{IL} = V_{th} \) and \( V_{IH} = V_{GS} \) at point B in Fig. 5-1(b)).

(d) (16 pt)
At which input state (ON or OFF), static power is consumed (i.e. current flows)? ON state: \( V_{GS} = V_{DD} \); OFF state: \( V_{GS} = 0 \). What is the output voltage \( (V_{OS}) \)? How much is the current? What is the average static power? (Hint: assume half of the period is operated at both ON and OFF states exactly.

6. Active filter: (29 pt)
For a feedback loop system shown in Fig. 6-1(a), the loop gain is \( L(s) = \frac{1}{1 + L(s)} \) and the characteristic equation is \( 1 + L(s) = 0 \). RC network \( r(s) \) is defined in Fig. 6-1 (b).

(a) (3 pt)
To get poles of the entire system with a characteristic equation above, you can actually calculate the zeros of the RC network. Please explain mathematically.

(b) (8 pt)
Please derive \( r(s) \) (\( = \frac{V_a}{V_b} \)) in terms of \( s \) for the circuit in Fig. 6-2.
(c) (6 pt)
You can translate the original feedback loop in Fig. 6-1 (a) to that in Fig. 6-3. Please show that these two loops are equivalent.

(d) (6 pt)
Based on the concept in (c), we can transform the circuit in Fig. 6-4 (a) to that in Fig. 6-4 (b). Please place the 4 components \((R_1, R_2, C_3, \text{ and } C_4)\) in the right position on Fig. 6-4 (b). Please place the negative and positive input symbols into the two input terminals of the OP AMP.

![Fig. 6-4](image)

(e) (6 pt)
Based on (d), by injecting an input signal from one of the ground terminal in Fig. 6-5, what type of the filter do you have? Low-pass or high-pass? Please explain.

![Fig. 6-5](image)