1. (17 %) For a MOS+BJT differential pair as shown in Fig. 1, the threshold voltage of NMOS $M_1$ is 0.5 V and the thermal voltage for BJT $Q_1$ is 25 mV. For $Q_1$, its $V_{BE}$ is equal to 0.625 V when $I_c$ = 100 μA. For the tail current source, let's assume it is an ideal one with 1 mA. Channel length modulation and Early effect can be neglected in calculation. Note that $R_L$=0.5 KΩ.

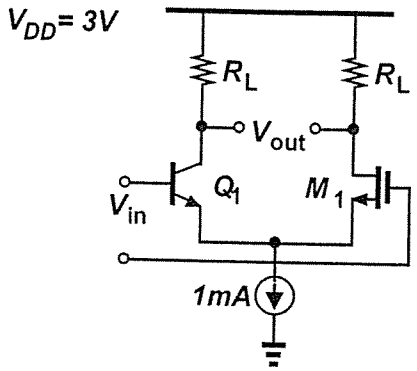


Fig. 1

(a) (6 %) Please design the size of $M_1$ and $V_{in}$ such that both $M_1$ and $Q_1$ draw the same current. Note that $\mu_n C_{ox}$=100 μA/V$^2$ and the voltage drop on current source is 200 mV.

(b) (6%) The design in part (a) yields an asymmetric pair. In order to design a fully differential circuit, the size of $M_1$ and $Q_1$ must be changed such that both $M_1$ and $Q_1$ have the same DC current bias and transconductance. Please calculate $(W/L)_{M1}$ and the number of $Q_1$ in parallel.

(c) (5 %) Please calculate the differential gain in part (b).

2. (33 %) In Fig. 2, neglect body effect in all transistors. Note that $(W/L)_{1,2}$=40/1, $(W/L)_{3,4}$=100/1 , $\mu_n C_{ox}$=50 μA/V$^2$ ,$\mu_p C_{ox}$=20 μA/V$^2$, $V_{An}$= 100 V, $|V_{Ap}|$= 66.67 V, $V_{tn}$= 0.5 V, and $V_{tp}$= - 0.5 V.

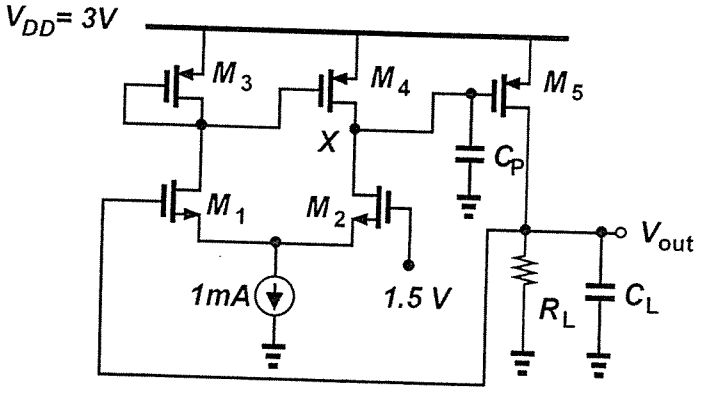


Fig. 2

(a) (11 %) First, you can neglect the channel length modulation such that the amplifier gain is infinite. Then, for $R_L$=75 Ω, what is the minimum and maximum $(W/L)_5$ such that all MOS transistors can operate in saturation region?

(b) (15 %) Now, let's choose $(W/L)_5$=3000 and assume the internal node X has total equivalent capacitance 1 pF, what is the value of $C_L$ (the total equivalent capacitance at $V_{out}$) to maintain the phase margin at 45 degree? In this case, we would like to have $V_{out}$ as the dominant pole. Also, please draw the small-signal model for this circuit.

(c) (7 %) Alternatively, we can design node X as the dominant pole. What is the maximum $C_L$ in this case to keep phase margin better than 45 degree?

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3. (25%) Given the quadrature oscillator circuit as shown below, answer the following questions.

(a) (5%) Show that the circuit involving the second OP amplifier is equivalent to a negative impedance converter, with equivalent impedance equal to $-R_f$ when looking into the right of the node marked with $v$.

(b) (5%) When $R_f$ is equal to 2R, show that the circuit at the right-hand-side of the output of the first OP amplifier acts as a non-inverting integrator.

(c) (5%) Without considering the output limiter circuit, derive the loop gain of the entire circuit and hence calculate the frequency of oscillation.

(d) (5%) Explain why the two output voltages at $v_{O1}$ and $v_{O2}$ have an exact phase difference of $90^0$.

(e) (5%) Explain the function of the limiter circuit in sufficient detail (5%).

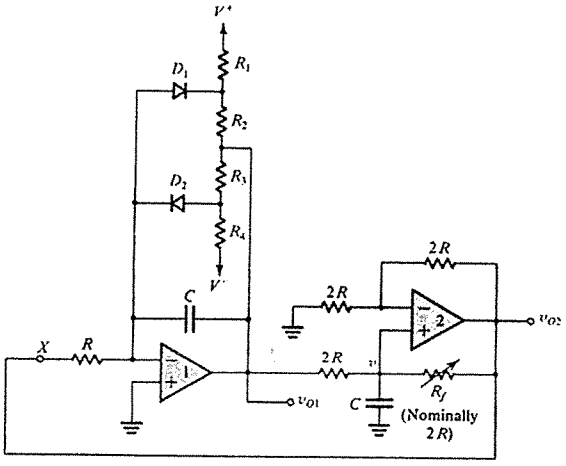


Fig. 3

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4. (25%) Given a static RAM cell based on the SR latch circuit shown in Fig.4a, the CMOS inverters are matched such that the circuit operation is symmetric around $V_{DD}/2$. Assume that the cell is storing a logic "0" in the output $Q$. A "set" operation by connecting $S$ to voltage $V_{DD}$ should ideally raise the voltage at the drain of $Q_5$ to at least $V_{DD}/2$ in order to trigger the regeneration via positive feedback. Here, assume for simplicity that the "set" operation involves only $Q_2$ and $Q_5$, and at the end of the "set" operation the condition is like that shown in Fig.4b.

(a) (5% each, total 10%) In what regions do the two transistors $Q_2$ and $Q_5$ operate?

(b) (5%) List the equation that equals the drain currents of $Q_2$ and $Q_5$.

(c) (5%) For the "set" operation to successfully trigger the switch, what is the minimum $W/L$ ratio of $Q_5$ relative to $Q_1$ (note: not relative to $Q_2$)?

(d) (5%) For a 0.18-μm fabrication process, with parameters $\mu_n C_{ox} = 4\ \mu_p C_{ox} = 300\ \mu A/V^2$, $V_{tn} = |V_{tp}| = 0.5$ V, $V_{DD} = 1.8$ V, plus the CMOS inverters $(W/L)_n = 0.27\ \mu m/0.18\ \mu m$ and $(W/L)_p = 4(W/L)_n$, calculate $(W/L)_5$ using a value at 1.5-fold of the minimum obtained from (c) for security.

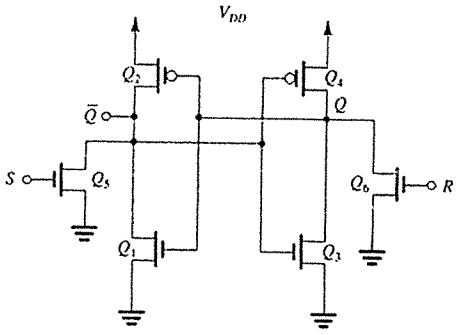


Fig. 4a

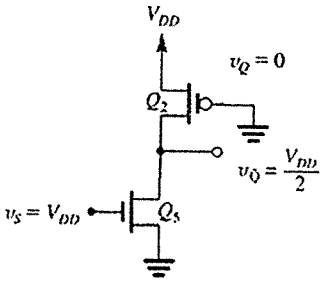


Fig. 4b

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