第一大題為複選選擇題，共 10 題，每題 4 分；第二大題為單選選擇題，共 5 題，每題 2 分。第一、二大題請作答於『答案卡』(請勿作答於試卷之選擇題作答區)，未作答於答案卡者，本大題不予計分。第三、四、五、六大題為非選擇題，請作答於『試卷』之非選擇題作答區。

一、複選選擇題 (40%)

1. Fig. 1 shows a 2-stage CMOS opamp. Which of the following(s) is (are) true? (A) Overall DC voltage gain=$g_{m1}(r_{o2}\|r_{o4})g_{m6}(r_{o6}\|r_{o7})$. (B) Dominant pole, $\omega_{p1}\sim=1/[(r_{o2}\|r_{o4})C_c g_{m6}(r_{o6}\|r_{o7})]$. (C) Unity-gain frequency, $\omega_t\sim=g_{m1}/C_c$. (D) If this opamp is connected as a unity-gain buffer, the closed-loop output resistance $R_{out}\sim=1/[g_{m6}g_{m1}(r_{o2}\|r_{o4})]$.

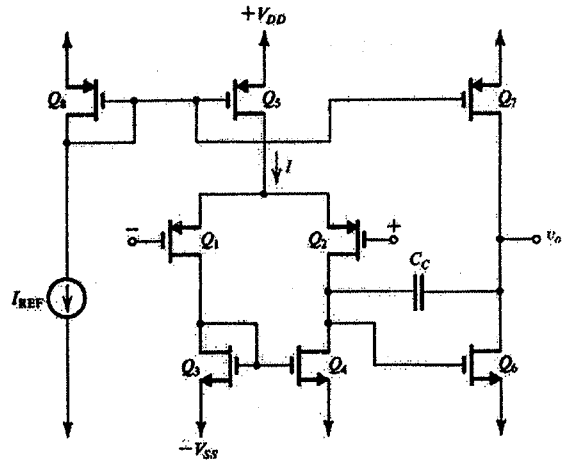

Fig. 1

2. Fig. 2 shows a first-order filter. Which of the following(s) is (are) true? (A) DC gain is $-R_2/R_1$. (B) The zero frequency is at $1/(2\pi R_2C_2)$. (C) HF gain is $-C_2/C_1$. (D) For $R_2C_2 < R_1C_1$, this filter shows a high-pass characteristic.

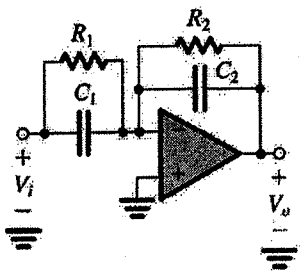

Fig. 2

3. In Fig. 3, Z_1 to Z_5 are passive components. In order for Z_{in} to show an inductive characteristic, which of the following(s) should be satisfied? (A) Z_1 is a capacitor, others are resistors. (B) Z_2 is a capacitor, others are resistors. (C) Z_3 is a capacitor, others are resistors. (D) Z_4 is a capacitor, others are resistors. (E) Z_5 is a capacitor, others are resistors.

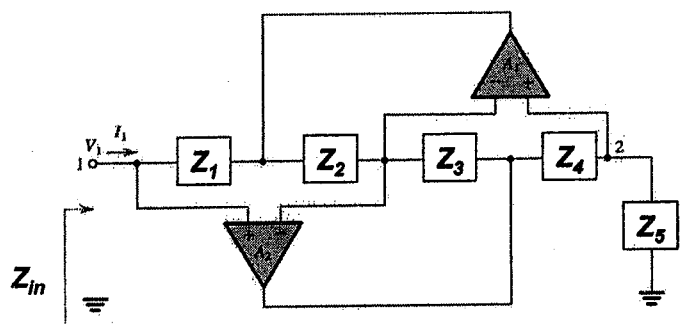

Fig. 3

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4. Fig. 4 show a biquad with feedforward. For C_1=0, R_2=∞, and R_3=∞, V_o is a negative band-pass signal. Which of the following(s) is (are) true? (A) This circuit is a KHN biquad. (B) This biquad can realize all second-order filter functions. (C) Changing either C_1, R_2, or R_3 will alter the poles of this biquad. (D) If C_1≠0, the numerator of the biquad transfer function will have a non-zero s^2 term. (E) If R_2 is a non-zero finite-valued resistor, the numerator of the biquad transfer function will have a non-zero s^1 term.

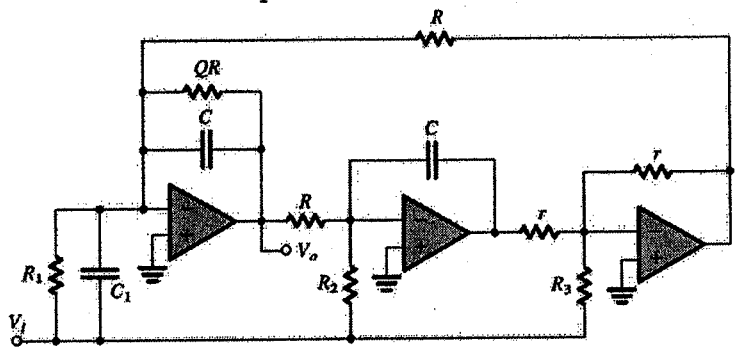

Fig. 4

5. Fig. 5 shows a switched-capacitor (SC) integrator. *S3* and *S4* are switches to be controlled by the clock signal. Which of the following(s) is (are) true? (A) Time constant of this SC integrator is $T_c \times C_2/C_1$. (B) If *S3* and *S4* are controlled by $\phi 1$ and $\phi 2$, respecitvely, this circuit realizes an inverting SC integrator. (C) If *S3* and *S4* are controlled by $\phi 2$ and $\phi 1$, respecitvely, this circuit realizes a non-inverting SC integrator. (D) This circuit topology is sensitive to stray cpacitance.

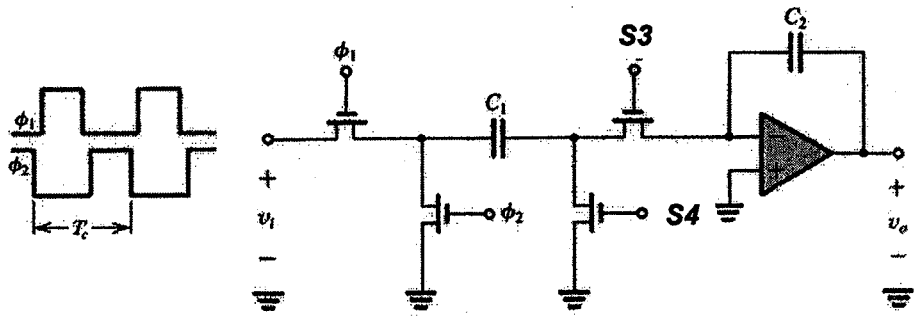

Fig. 5

6. Fig. 6 is an oscillator circuit. Which of the following(s) is (are) true? (A) In theory, the oscillator will start at any values of r_2 and r_1. (B) The oscillator frequency is determined by $\omega_0 = 1/(LC)^{0.5}$. (C) The oscillator has a self-limiting mechanism to stabilize the oscillation amplitude. (D) With r_2=0, the oscillator can start successfully.

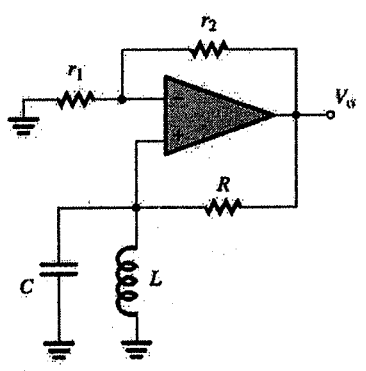

Fig. 6

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7. In Fig. 7, all transistor sizes are chosen to match the delay of a basic CMOS inverter with $(W/L)_n=n$ and $(W/L)_p=p$. To meet this goal, which of the following transistor sizing condition(s) should be adopted? (A) $Q_{NA}=n$, $Q_{NB}=2n$, $Q_{NC}=n$, $Q_{ND}=n$. (B) $Q_{NA}=n$, $Q_{NB}=2n$, $Q_{NC}=2n$, $Q_{ND}=2n$. (C) $Q_{PA}=3p$, $Q_{PB}=1.5p$, $Q_{PC}=3p$, $Q_{PD}=3p$. (D) $Q_{PA}=3p$, $Q_{PB}=3p$, $Q_{PC}=3p$, $Q_{PD}=1.5p$.

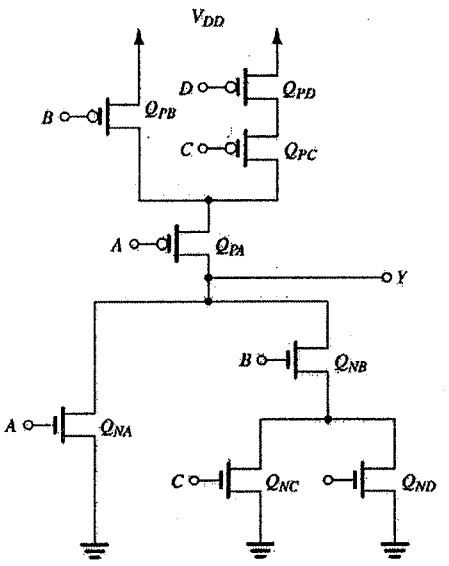

Fig. 7

8. Fig. 8(a) and Fig. 8(b) show two NMOS circuits. Which of the following(s) about these circuits is (are) true? (A) In Fig. 8(a), when $v_I=0$, v_O reaches V_{DD}. (B) In Fig. 8(a), when $v_I=V_{DD}$, v_O is low and is independent of sizes of Q_1 and Q_2. (C) In Fig. 8(b), since the V_{GS} of Q_2 is 0, Q_2 is turned off. (D) The circuit of Fig. 8(b) can possibly operate as an inverter. (E) It requires an extra process step to fabricate the transistor Q_2 of Fig. 8(b).

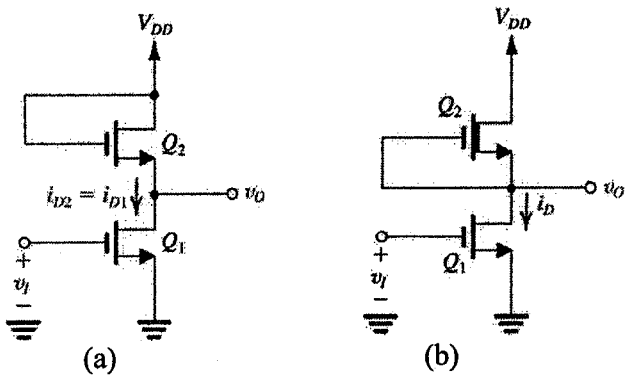

Fig. 8

9. Fig. 9 shows a simple pass-transistor logic (PTL) circuit using NMOS as a switch. Which of the following(s) about this circuit is (are) true? (A) If $v_I=V_{DD}$, then $v_O=V_{DD}$. (B) If $v_I=0$, then $v_O=0$. (C) Transistor Q suffers from the body effect when passing a logic '1' signal from v_I to v_O. (D) Transistor Q suffers from the body effect when passing a logic '0' signal from v_I to v_O. (E) This circuit requires special techniques to restore the value of V_{OH} to V_{DD}.

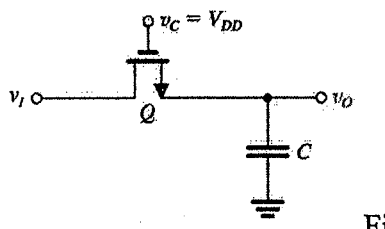

Fig. 9

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10. Which of the following(s) about the dynamic logic circuit shown in Fig. 10 is (are) true? (A) $V_{OH}=V_{DD}$ and $V_{OL}=0$. (B) The values of V_{IH} and V_{IL} depend on transistor sizings. (C) NM_H is lower than NM_L. (D) Cascading multiple dynamic logic circuits may lead to errornous output due to premature capacitor discharge. (E) This is a static logic circuit.

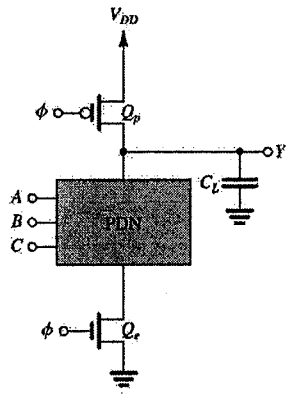

Fig. 10

二、單選選擇題 (10%)

11. Fig. 11 shows a 6T-SRAM circuit. Before the read operation, both lines (B and $\overline{B}$) are precharged to V_{DD}. Assume a logic '0' is stored in this cell (Q=0). Which of the following about the SRAM cell operation is true? (A) After the Word line is activated, Q_5 and Q_6 turns on; the voltage at node Q will be increased to near V_{DD}. (B) The readout process is destructive. (C) To write a '1' into the cell, B line is raised to V_{DD}. Once Q_6 turns on, the voltage at node Q will be rasied to near V_{DD} immediately. (D) The write process is faster than the read process.

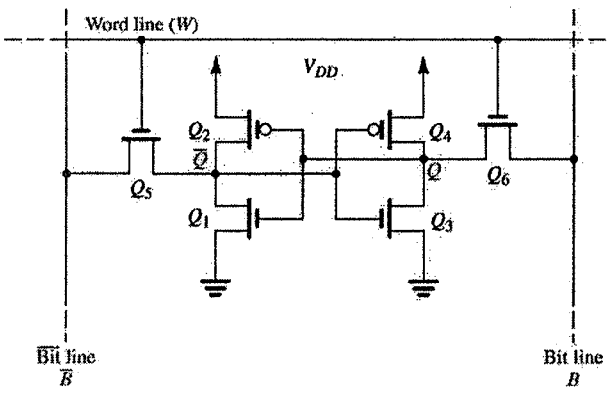

Fig. 11

12. Which of the following about a DRAM is true? (A) The DRAM cell must be refreshed periodically. (B) It is a type of read-only memory. (C) It is a non-volatile memory. (D) The readout process of a DRAM is non-destrctive.
13. Which of the following about the negative feedback is true? (A) It increases the closed-loop gain. (B) It increases the gain-bandwidth product. (C) It hels to reduce nonlinear distortion. (D) It can be utilized to design an oscillator.
14. A general form of a second-order circuit can be expressed as $T(s) = (a_2s^2+a_1s+a_0)/(s^2+b_1s+b_0)$. Which of the following is NOT true? (A) If the two poles are complex-valued, they must be complex-conjugate poles. (B) For the circuit to be stable, the ploes must be in the left half of the s-plane. (C) A circuit with right-half plane poles subjecting to a disturbance will show an oscillation with decaying amplitude. (D) The poles of a stable oscillator lies in the $j\omega$ axis of the s-plane.

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15. Which of the following about the CMOS logic-gate circuit is NOT true? (A) It does not consume static power. (B) The operation of a CMOS logic circuit does not require a clock signal. (C) Under matched condition, V_M=0.5×V_{DD}. (D) It is possible that the pull-up network (PUN) and the pull-down network (PDN) are not dual networks. (E) Values of V_{OH} and V_{OL} depend on device sizing.

第三、四、五、六大題為非選擇題，請於試卷上作答。

三、For the following amplifier (Fig. 12), v_I = 10 mV, i_I = 1 mA, v_O = 1 V, i_O = 10 mA, what is the amplifier's power gain in dB? (10%)

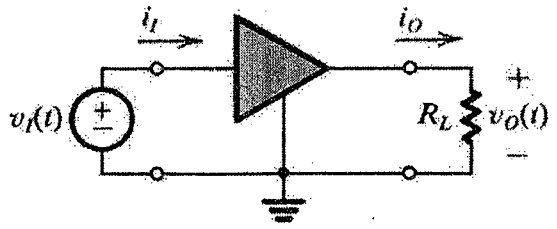

Fig. 12

四、Draw the complete circuit schematic diagram of a PMOS common-gate amplifier with the open-circuit voltage gain of g_mR_D. **All the terminals** of the transistor and their connection need to be shown explicitly. The input and output terminals of the amplifier also need to be indicated. The supply voltage is V_S and the bias voltage is V_b. Note: No partial credit will be given. (10%)

五、For the following circuit (Fig. 13), Q_4–Q_6 has a transmission factor of 6 [i.e., $(W/L)_6/(W/L)_4 = 6$], Q_3–Q_5 has a transmission factor of 1, and Q_7–Q_8 has a transmission factor of 6. All transistors are sized to operate at the same overdrive voltage, $|V_{OV}|$. All transistors have the same Early voltage $|V_A|$.

(a) Find the differential voltage gain, A_d. (5%)

(b) Find the common-mode voltage gain, $|A_{cm}|$ assuming the output resistance of the bias current source I is R_S. (5%)

(c) Find CMRR in terms of $|V_A|$ and $|V_{OV}|$. (5%)

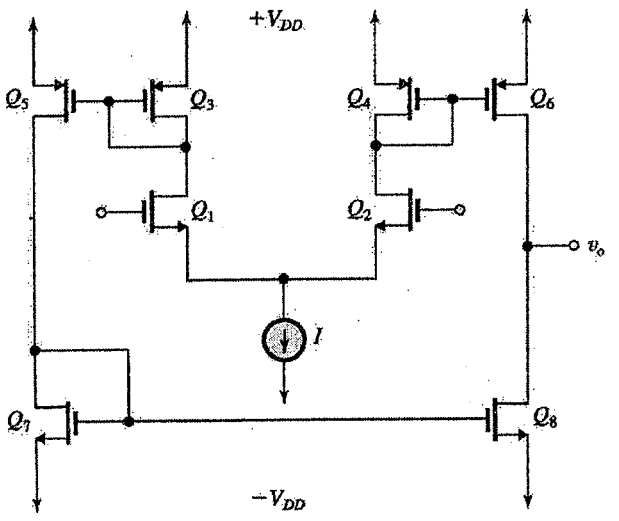

Fig. 13

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六、For the following amplifier (Fig. 14), g_m = 1.5 mA/V, C_{gs} = 10 fF, C_{gd} = 2 fF, C_L = 20 fF, R_S = 10 kΩ, and R_D = 10 kΩ. Determine f_H and frequency of the transmission zero f_Z caused by C_{gd}. (15%)

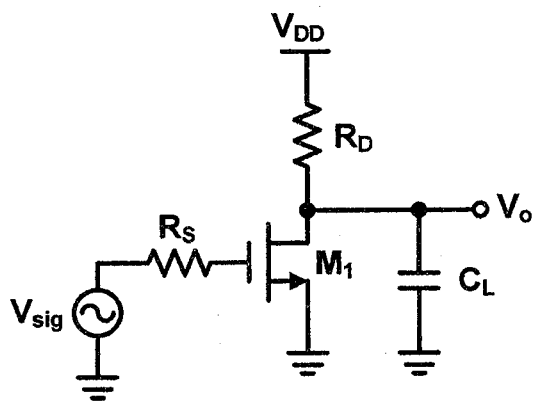

Fig. 14

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