1. For the circuits shown in Fig. 1, assuming that the opamps are ideal.
   (a) For Fig. 1(a), derive an expression for the differential voltage gain, V_{out}/V_{in}. (10%)
   (b) In Fig. 1(b), let $C_2 = C_4 = C$, $C_1 = 10C$, $C_3 = 8C$, and $R_1 = R$, please derive an expression for the differential voltage gain, V_{out}/V_{in}. (10%)
   (c) Plot the frequency response of the voltage gain (V_{out}/V_{in}) derived in (b). You must denote key parameters in the plot. (10%)

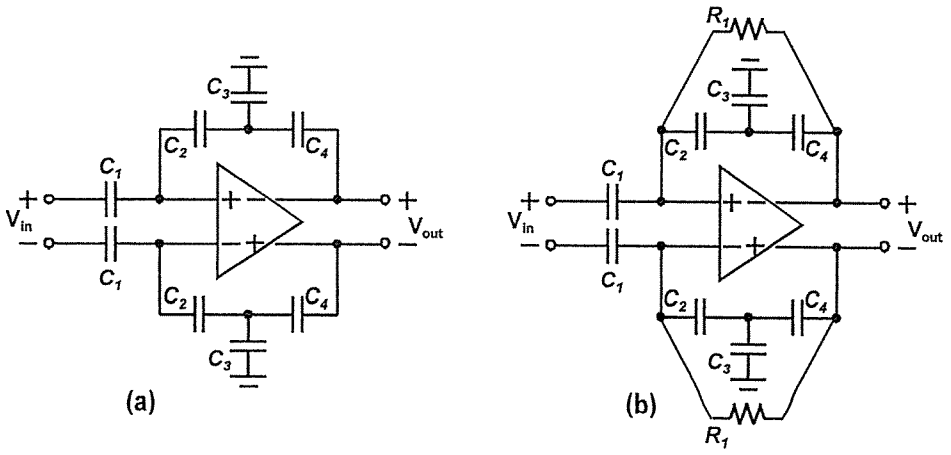

Fig. 1

2. Please refer to Fig. 2.
   (a) For the circuit of Fig. 2(a), it consists of 2 trans-conductors and a capacitor. Please derive an expression for its input impedance, Z_{in}. What is the purpose of this circuit? (10%)
   (b) For the circuit of Fig. 2(b), assuming V_b, I_1, and I_2 are chosen appropriately such that this circuit is properly biased. Considering transistor parasitic capacitance, but ignoring the channel-length modulation effect, please derive an expression for the input impedance, Z_{in}. (10%)
   (c) Next, derive an expression for the input impedance, Z_{in}, when channel-length modulation effect is considered. How does this affect the circuit performance? (10%)

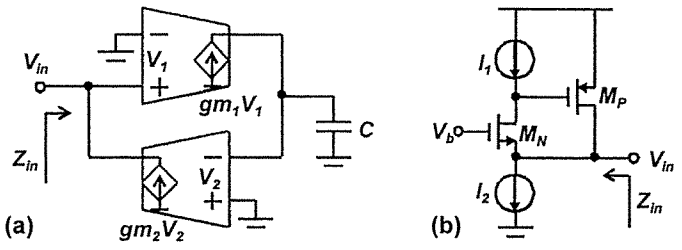

Fig. 2

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3. Fig. 3 depicts an SRAM cell.
(a) Describe the **Read** operation of the SRAM cell. Please draw related timing waveforms to assist your description. (5%)
(b) Describe the **Write** operation of the SRAM cell. Please draw related timing waveforms to assist your description. (5%)
(c) How are the sizes of access transistors (Q_5/Q_6), NMOS transistors (Q_1/Q_3), and PMOS transistors (Q_2/Q_4) determined? Please discuss the design guidelines. (10%)

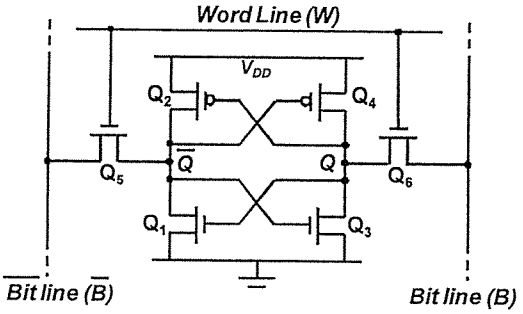

Fig. 3

4. Fig. 4 depicts an amplifier circuit.
(a) Derive expressions for the voltage gain, $V_{out}/(V_2 - V_1)$, and the output resistance, R_{out}. (10%)
(b) This circuit has the following parameters: I_{bias} = 0.2 mA, V_{DD} = 3 V, R_1 = 2 kΩ; NMOS parameters are: K_n = 4 mA/V^2, V_{TN} = 1 V, V_A = 40 V; PMOS parameters are: K_p = 1 mA/V^2, V_{TP} = -1V, V_A = 25 V. Calculate the voltage gain and output resistance derived in (a). (5%)
(c) What may be the purpose of adding two resistors (the two R_1) to this circuit? What are the penalties by doing so? (5%)

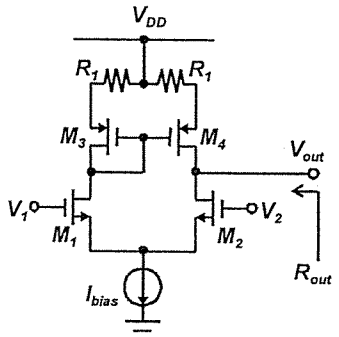

Fig. 4

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