※選擇題部分請作答於電腦答案卡上，並且限用 **2B** 鉛筆。

(60 pts，4pts. each)選擇題共 15 題，可能有一個以上的答案，全對才給分，請於答案卡上作答。

1. The function of the circuit in Fig. 1 is: (A) an 8-T SRAM; (B) a Domino buffer; (C) an oscillator with a reset control line; (D) a clocked SR flip-flop; (E) none of the above.

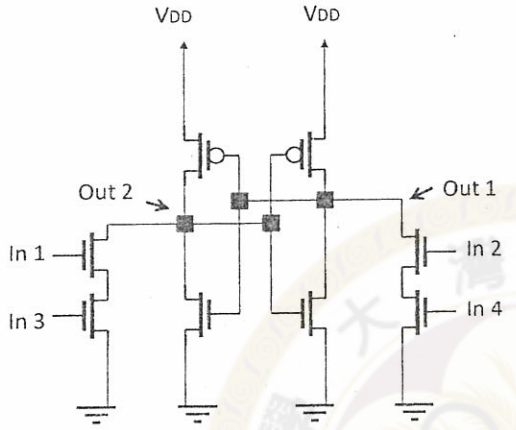

Fig. 1

2. Refer to Fig. 2, assume that the electron and hole mobilities of the device are 450 ($cm^2/V \cdot s$) and 150 ($cm^2/V \cdot s$), respectively. Assume that the NMOS width = 80 nm and NMOS length = 40 nm in the basic CMOS inverter, if the worst-case gate delay is equal to that of the basic inverter, which of the following are true?
(A) The width and length of QP1 should be 240 nm and 40 nm, respectively;
(B) The width and length of QP1 should be 160 nm and 40 nm, respectively;
(C) The width and length of QN3 should be 160 nm and 40 nm, respectively;
(D) The width and length of QN1 should be 80 nm and 40 nm, respectively;
(E) None of the above.

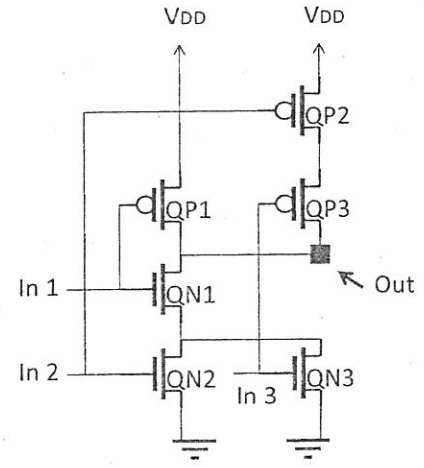

Fig. 2

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3. Refer to Fig. 3, for a triangular/square waveform generator, which of the following are true? (A) The resistor, R, is connected to the noninverting input of the OP-AMP; (B) The bistable circuit is of the inverting type; (C) A square waveform can be measured at the point Vx; (D) The positive slope of the triangular waveform is equal to Lp/(RC); (E) None of the above.

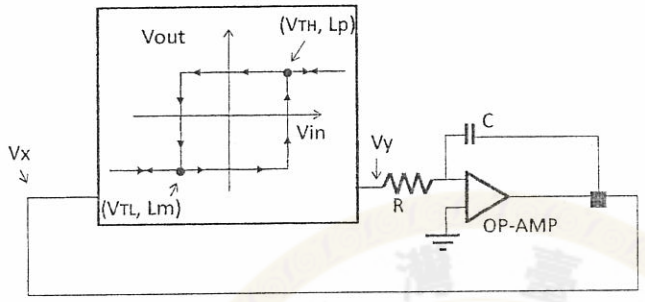

Fig. 3

4. When comparing the devices of 130 nm CMOS technology with the devices of 350 nm CMOS technology, a 130 nm device usually has: (A) a thinner oxide layer; (B) a lower channel doping concentration; (C) a smaller unit-gain frequency; (D) a smaller effective mobility; (E) none of the above.

5. Select the correct statement(s):
(A) Current mirror is an ideal circuit source;
(B) The larger the slew rate, the better the design;
(C) The larger the stage number of a ring oscillator, the higher the frequency it oscillates at;
(D) The lower the ambient temperature, the better the circuit performs;
(E) None of the above.

6. Select the correct statement(s):
(A) The light-emitting diodes are usually forward-biased;
(B) The photodiodes are usually reversely-biased;
(C) Varactors are usually made of reverse-biased pn junctions;
(D) Schottky-barrier diodes (SBD) operate faster than pn-junction diodes because SBD have heavily doped ohmic contacts;
(E) None of the above.

7. Pick the correct statement(s):
(A) Permittivity of free space is 8.85×10^{-14} J/cm;
(B) Boltzmann constant is 8.62×10^{-5} Kg/s;
(C) Magnitude of electron charge is 1.602×10^{-19} C;
(D) 1 Watt is equal to 1000 Joule/sec;
(E) None of the above.

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8. Assume that the thermal voltage is 0.026V, given $n_i = 1.5x10^{10}/cm^3$, for a silicon pn junction with $N_A = 10^{18}/cm^3$, $N_D = 10^{17}/cm^3$, junction area = $80\mu m^2$, and the reverse-biased voltage V_R= 1V; Which of the following are true?
(A) The built-in voltage is about 877mV;
(B) The width of the depletion region of an open-circuited junction is 0.16 μm;
(C) The depletion capacitance at V_R= 1V is larger than 100 pF;
(D) The depletion capacitance at V_R= 1V is smaller than 0.1 pF;
(E) None of the above.

9. For a NMOS transistor, its threshold voltage will _____ as temperature increases
(A) increase (B) decrease (C) remain unchanged (D) all of the above are possible.

10. For a MOS differential pair in Fig. 4, node *X* can become virtual ground if
(A) all transistors are matched (B) input are fully differential (C) M_b are in saturation region (D) all of the above.

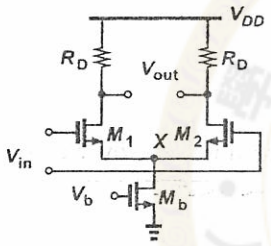

Fig. 4

11. For a given feedback system, when we increase the feedback factor, what will we get?
(A) higher close-loop gain (B) faster response (C) large linear input range (D) more stable close-loop gain.

12. For a MOS circuit with dual power supplies, V_{dd} (>0) and V_{ss} (<0), what should the p-substrate be connected to?
(A) V_{dd} (B) V_{ss} (C) GND(=0V) (D) all of the above are possible

13. For a MOSFET current source, we can cascode a MOS shown in Fig. 5 to get
(A) higher current output (B) higher output impedance (C) smaller temperature variation (D) all of the above

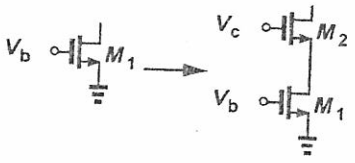

Fig. 5

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14. For a common-emitter amplifier circuit shown in Fig. 6 what's the maximum gain we can obtain? Please use $V_{CE,SAT}$=0 for this question
(A) V_{cc}/V_T (B) V_{cc}*q/kT (C) $V_{cc}/(I_c*R)$, I_c is the collector current of Q_1(D) none of the above

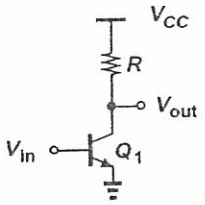

Fig. 6

15. For a common-drain circuit, its low-frequency gain can be
(A) larger than unity (B) smaller than unity (C) 10 (D) all of the above are possible

(40 pts)以下為計算題，共兩大題

1. (20pts)Given the transfer function of a filter, $T(S) = {}^{3}/_{(2S^3 + 4S^2 + 4S + 2)}$, answer the following questions:

(a) (6 pts) List all the pole(s) and zero(s) in the unit of ***rad/s***.
(b) (6 pts) Draw the pole-zero pattern of the filter. Is this a high-pass filter or a low-pass filter (or neither)?
(c) (4 pts) Calculate the magnitude function of the filter, $|T(j\omega)|$.
(d) (4 pts) Calculate the ω_{3dB}.

2. (20 pts) The circuit in Fig. 7 contains a two-stage BJT CE amplifier with its bias circuit. Note that β=100 for all BJTs, in which Q_0 to Q_2 have the same I_s. Q_3 has scale current I_{s3}(=3I_s) and Q_4 has scale current I_{s4}(=5I_s). To simplify calculation, you can neglect base-width modulation and can assume C_1 to C_3 is quite large. Note that all BJTs are in forward-active region. Please use V_T=25 mV and V_i is an AC voltage source only.

(a) (5 pts) Please calculate R_0 so that $I_{c3}+I_{c4}$=8 mA.
(b) (7 pts) Draw the small-signal model for this two-stage amplifier.
(c) (8 pts) Now, $R_{B1}=R_{C1}=R_{B2}=R_{C2}$=2KΩ Calculate V_{out}/V_i.

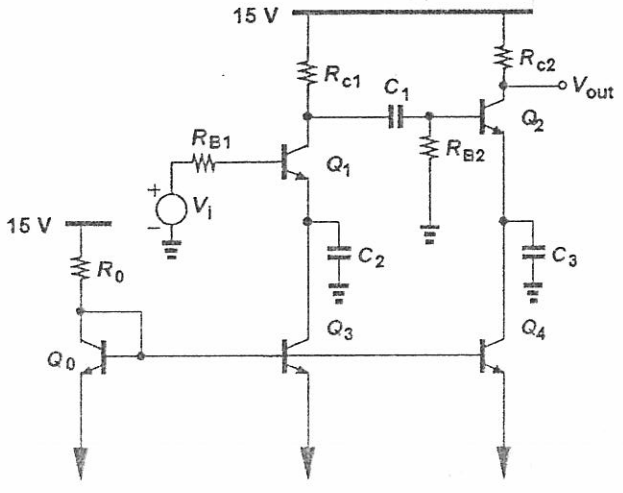

Fig. 7

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