國立臺灣大學99學年度碩士班招生考試試題

1. Both of the MOSFET and BJT are widely used in circuit design. Therefore, it is quite important to understand the operation-principle of these devices. Please answer the following questions with few sentences and schematics if necessary.
   (a) Please draw the cross-section of NMOS-FET and pnp BJT and denote the terminal of each device. (6%)
   (b) What is the carrier mainly conducting the current in each device drawn in (a)? (4%)
   (c) What is the major carrier-movement mechanism in each device drawn in (a)? (4%)
   (d) Please name one breakdown mechanism of each device drawn in (a) and briefly explain the mechanism. (6%)
   (e) Which one of the MOSFET and BJT is more vulnerable to temperature effect? (2%)
   (f) Both of MOSFET and BJT have the characteristic of "early voltage." However, the phenomenon is resulting from different effect. Please briefly explain the causes of the "early voltage" in both MOSFET and BJT. (4%)

2. The circuit symbols in Figure 1a are a ***PMOS***, an ***NMOS***, and an inverter, ***Ckt_Inv***, respectively.
   (a) (5%) Which is the correct statement? The circuit, ***Ckt_1***, in Figure 1b is:
      (1) A positive-edge triggered D flip-flop;
      (2) A negative-edge triggered D flip-flop;
      (3) A transparent latch;
      (4) A ring oscillator;
      (5) None of the above.
   (b) (5%) Which is the correct statement? The circuit, ***Ckt_2***, in Figure 1c is:
      (1) A source follower;
      (2) A shift register;
      (3) An SRAM cell;
      (4) A multiplexer;
      (5) None of the above.
   (c) (15%) Please design a dual-edge triggered flip-flop.

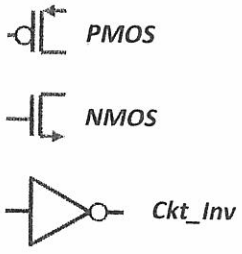

Figure 1a: symbols

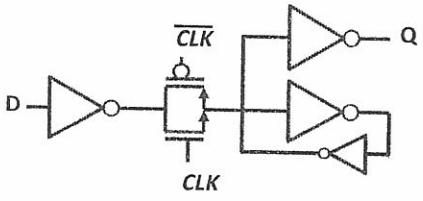

Figure 1b: ***Ckt_1***

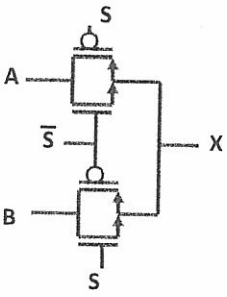

Figure 1c: ***Ckt_2***

3. Consider the differential amplifier shown in Figure 2.
   (a) Assume the op amp is ideal. Please derive the closed-loop gain of this amplifier (5%)
   (b) Assume the op amp is ideal and resistors are perfect. What is the condition to obtain the differential amplifier with CMRR→∞ (2%)
   (c) Assume the op amp has a finite open-loop gain. Please derive the closed-loop gain of this amplifier (6%)

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(d) Assume R1=1kΩ; R2=10kΩ; R3=2kΩ; and R4=20kΩ and the op amp is ideal. In addition, $V_1(t)=\sin(2\pi t)$ V and $V_2(t)=\sin(2\pi t+\pi)$. Please draw the output voltage waveform for $0 \leqq t \leqq 2$ (5%)

(e) Because of the low input resistance, the usage of this differential op amp configuration is limited. Please derive the differential input resistance of the op amp configuration and explain the reason why it becomes a problem in differential amplifier configuration. (6%)

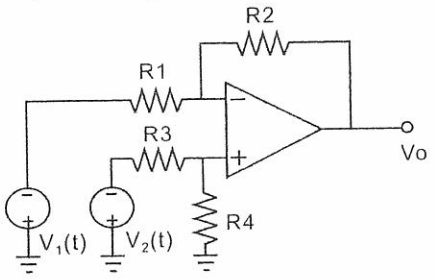

Figure 2.

4. As shown in Figure 3.

(a) (5%) Which is the correct statement? The circuit in Figure 3 is usually referred as:

(1) A transimpedance amplifier;

(2) A feedback amplifier;

(3) A voltage amplifier;

(4) A two-stage amplifier;

(5) A unity-gain amplifier.

(b) (5%) What is the output pole of the circuit?

(c) (15%) Please calculate V_{out}/I_{in} in Figure 3. You have to include all parasitic capacitance, output resistance, transconductance, and body effect in the analysis.

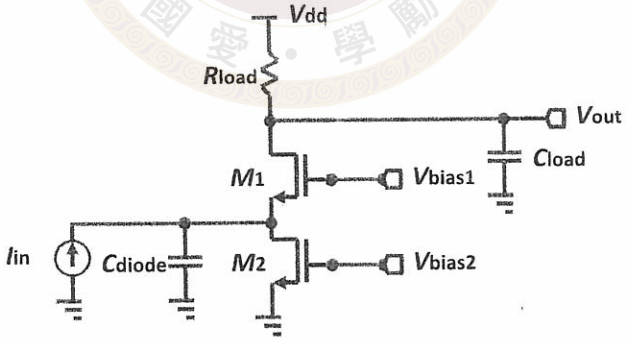

Figure 3.

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