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國立臺灣大學 102 學年度碩士班招生考試試題

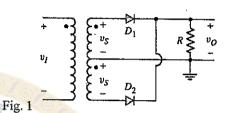
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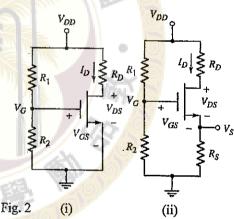
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1. (30%) (a) Please explain why it is usually encouraged to adopt the strategy of cascaded amplifiers? (b) In your opinion, what is the most important property desired for the first (input) stage amplifier? (c) In your opinion, what is the most important property desired for the output stage? (d) Please use one BJT transistor and a couple of resistors to design a buffer amplifier. (e) Please provide the small-signal equivalent circuit for your buffer amplifier. (f) Please specify the input and output resistance for your buffer amplifier. (g) Please specify the voltage gain of your buffer amplifier.

- 2. (15%) Consider a rectifier circuit in Fig. 1, where v<sub>I</sub> is a sinusoidal input signal with a peak voltage of 120V and a frequency of 60 Hz. The transformer has a turns ratio of N<sub>1</sub>: N<sub>2</sub> = 8: 1, where N<sub>2</sub> is the number of turns on each of the secondary windings to produce both v<sub>S</sub>. Assume the diode cut-in voltage is 0.7 V and the output resistance is 2.5 kΩ. A filter capacitor, C, is connected in parallel with R. If the ripple of the output voltage is limited to 1 V (peak to peak), (a) determine the minimum value of the capacitance C; (b) Please explain how a regulator composed of diodes can be used to further reduce the ripple of the output.
- 3. (20%) The MOSFET transistor in the circuits shown in Fig. 2(i) and (ii) has parameters  $V_T = 1$  V and  $K_n'(W/L) = 2$  mA/V<sup>2</sup>. The circuit is biased with  $V_{DD} = 8$  V. Let  $R_1 + R_2 = 800 \text{ k}\Omega$ . (a) Design the circuit in Fig. 2(i) such that  $I_D = 0.64$  mA and  $V_{DS} = 4$ V; (b) Now consider the circuit in Fig. 2(ii). Redesign the circuit with  $R_D = R_S$  to achieve the same values of  $I_D$  and  $V_{DS}$ ; (c) Which design is better? Why? (d) Use the small-signal model of the MOSFET to calculate the input resistance  $R_{in}$ , the voltage gain  $A_{v_i}$ , and the output resistance  $R_{out}$  of the circuits in Fig. 2(i) and (ii) respectively.
- 4. (15%) In the amplifier circuit of Fig. 3, the signal is applied to the source of  $M_1$  and the output is at the drain of  $M_1$ . (a) Please first derive the small-signal equivalent circuit of Fig. 3. (b) Determine the small-signal voltage gain and output resistance of this amplifier circuit.
- 5. (20%) A difference amplifier is one that responds to the difference between the two signals applied at its input and ideally rejects signals that are common to the two inputs. Please use at most three operational amplifiers (op amp) and some resistors (only two values, 10 kΩ and 1 MΩ, are available) to design a difference amplifier. Your difference amplifier is expected to have a differential gain larger than 10,000 and an ideal common-mode gain of 0. Also, an input resistance of larger than 1 MΩ is required at each of the inputs.





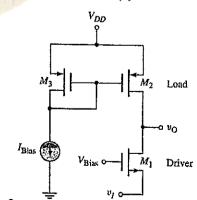


Fig. 3