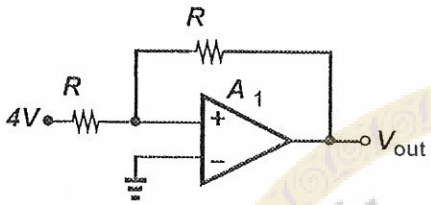
國立臺灣大學101學年度碩士班招生考試試題

(50 pts，5pts. each)選擇題共 10 題，可能有一個以上的答案，全對才給分。

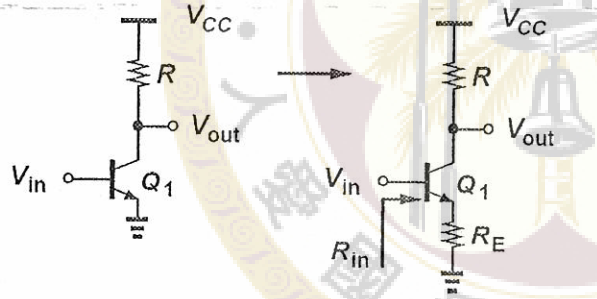
※ 注意：請用 2B 鉛筆作答於答案卡，並先詳閱答案卡上之「畫記說明」。

1. For an NPN transistor with a constant current on it, its V_{BE} will _____ as temperature increases
(a) increase (b) decrease (c) unchanged (d) all of the above are possible

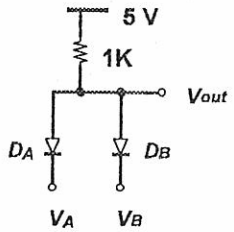
2. For a op amp circuit as follows, what is V_{out}? Assume op amp A_1 has the max/min output voltage at 10V/-10V.
(a) 4V (b) -4V (c) 10V (d) -10V (e) can not be determined.



3. For a common-emitter (CE) amplifier with emitter degeneration, which of the following statements are TRUE compared with CE amplifier without emitter degeneration? Assume both circuits have the same loading and DC bias current.
(a) higher gain (b) better linearity (c) wider 3-dB bandwidth (d) lower input resistance (R_{in}) (e) None of the above.



4. For a diode circuit as follows, Note that $I_S=10^{-14}$ A for both diode and $V_T=kT/q=25$ mV. Also, in didoe I-V equation, use n=1 in this case. In the circuit, $V_A=(2+\Delta v)$ Volt and $V_B=(2-\Delta v)$ Volt. Now, what Δv can make $I_{DB}/I_{DA}=100$?
(a) $\Delta v < -30$ mV (b) $\Delta v < -60$ mV (c) $\Delta v < 30$ mV (d) $\Delta v < 60$ mV (e) all of the above are possible



5. For a MOSFET common-source amplifier, we can cascode a MOS shown in Fig. 5 to get ____. Assume R_D is quite small compared with r_o of MOSFET.
(a) 10X small-signal gain (b) less Miller effect for C_{gs} in M_1 (c) larger output-swing for a given power supply and loading (d) higher R_{out} (e) all of the above

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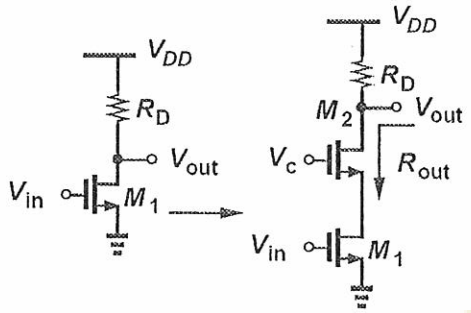
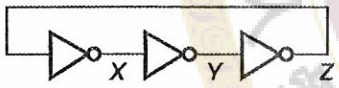


6. Which of the following statements is incorrect? (a) a feedback loop can desensitize gain; (b) an unstable system encloses the (-1,0) point in its Nyquist plot; (c) a stable system has no pole located in the right-hand side of *s*-plane; (d) a feedback system can reduce noise.

7. Which of the following statements is incorrect? (a) differential circuits can suppress common-mode noise; (b) source/emitter degeneration reduces gain; (c) source/emitter degeneration degrades linearity; (d) source/emitter degeneration improve matching between current sources.

8. Consider the following three stage ring oscillator, which one is its large signal oscillation frequency (T_D is gate delay of the ring oscillator)? (a) $2\pi/2T_D$ (b) $2\pi/3T_D$ (c) $2\pi/6T_D$ (d) $2\pi/9T_D$



9. Which of the following statements is correct? (a) pseudo-NMOS circuit family has better speed and power performance indices for large-scale digital systems; (b) noise margin (i.e. NMH and NML) for a certain circuit family is fixed and can't be adjusted by modifying transistor's widths;
(c) in current CMOS process technologies, copper is used for metal layers because of better conductivity; (d) skin effect implies that effective conductive area will be reduced for lower frequency signals through metal layers.

10. Which of the following statements is(are) incorrect? (a) in "dynamic logic circuit", a dynamic gate can not drive another, because output is monotonic during evaluation; (b) in "pass-transistor logic circuit", the NMOS switch can deliver a "good 1", and the PMOS switch can deliver a "good 0"; (c) SR flip-flop circuit is level sensitive; (d) read only memories retain their contents when power is removed.

接次頁

(50 pts)以下為計算題，共兩大題

※ 注意：請於試卷內之「非選擇題作答區」依序作答，並應註明作答之大題及小題題號。

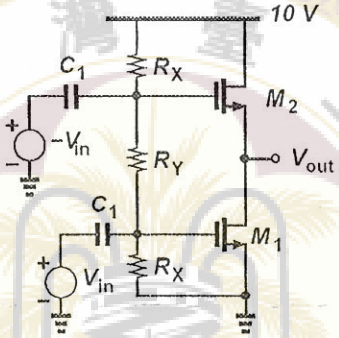
1. (25 pts) The following circuit contains a two-MOS transistor-circuit. Both transistors, M_1 and M_2, have (W/L)=20. Use $\mu_n C_{ox}$=0.1mA/V^2 and V_{tn}=1V. Neglect body effect and channel length modulation.

(a) (5 pts) Please calculate V_{g1} (gate voltage of M_1) so that I_{d1}=1 mA. For now, you can assume M_1 in saturation region.

(b) (3 pts) Derive the ratio of R_x to R_y to obtain the answer in (a).

(c) (10 pts) Draw the small-signal model and derive V_{out}/ V_{in} in low frequency. Let's assume V_{in} is an AC source. You don't need to consider the parasitic capacitance of transistors. Also, assume C_1 is very large.

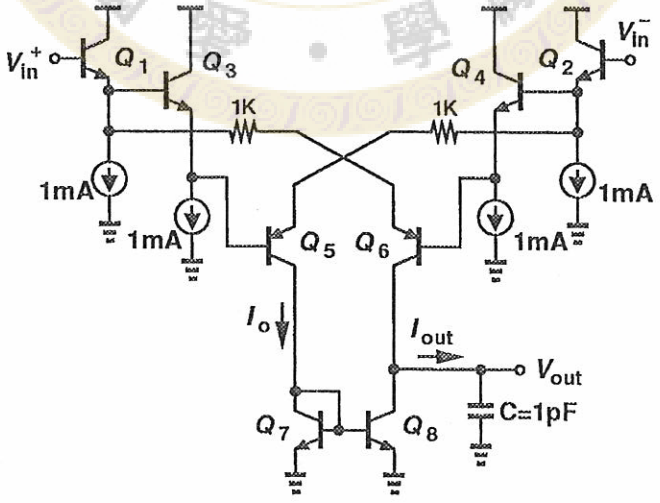
(d) (7 pts) What's the amplitude range of V_{in} such that both of M_1 and M_2 can keep in saturation region?



2. (25 pts) Consider the following symmetric circuit with current mirroring sources Q_7 and Q_8. All transistors are biased in forward active with r_o = 10 kΩ. $V_{in} = V_{in}^+ - V_{in}^-$

(a) Determine the bias current I_o when V_{in} = 0. (7%)

(b) Calculate the small-signal gain V_{out} / V_{in}. (8%)



(c) If $V_{in}(t) = \begin{cases} 2, & t \geq 0 \\ 0, & t < 0 \end{cases}$, estimate the output current I_{out} for $t \geq 0$. (10%)

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