國立臺灣大學99學年度碩士班招生考試試題

1. (15%) You are given a three-stage amplifier. The original overall upper 3-dB frequency is 2 MHz. What can you do if your boss asks you to lower the overall upper 3-dB frequency to 10 kHz?
2. (10%) Please design a differentiator using an ideal op amp, a 10-kΩ resistor, and a 0.01-μF capacitor. Specify the time-constant of the differentiator. Please explain why differentiator circuits are generally avoided in practice.
3. (15%) Please design a full-wave rectifier circuit to provide an average output voltage of 10V on which a maximum of ±1-V ripple is allowed. What else can you do to further reduce the ripple into ±0.1-V?
4. (10%) Please design a source follower using a *p*-channel enhancement MOS transistor. Specify the open-circuit voltage gain and the output resistance of your circuit.
5. (15%) You are asked to create a BJT amplifier with a transconductance of 50 mA/V and a base input resistance of 2000 Ω or more. Please describe at least two ways by which you can bias the circuit. What is the minimum β (common-emitter current gain) you can tolerate for the transistor used?
6. (10%) Describe a three-input CMOS OR logic circuit. What are the advantages of using CMOS circuits when compared to NMOS logic circuits?
7. (10%) How is a junction capacitance created in a reverse-biased *pn* junction diode?
8. (15%) Design a summing amplifier to produce 100 times of the average (magnitude) of three input voltages using op amps and resistors. The maximum possible resistance is 1 MΩ. Please have each input signal sees the maximum possible input resistance.

試題隨卷繳回