1. Consider the circuit in Fig. 1, $V_{DD} = V_{SS} = 10$ V, $I = 0.5$ mA, $R_G = 4.7$ MΩ, $R_D = 15$ kΩ, $V_t = 1.5$ V, and $k_n'(W/L) = 1$ mA/V^2. **(15%)**
(a) Find V_{OV}, V_{GS}, V_G, V_S, and V_D. (5%)
(b) Calculate g_m and r_o assuming that $V_A = 75$ V. (3%)
(c) What is the maximum possible signal swing at the drain for which the MOSFET remains saturation? (2%)
(d) Use this circuit and ground the gate as the common-gate amplifier, find R_{in} (input resistance), R_{out} (output resistance), A_{vo} (open-circuit voltage gain), A_v (voltage gain), and G_v (overall voltage gain) for the load resistance $R_L = 15$ kΩ, and $R_{sig} = 50$ Ω, where R_{sig} is the internal resistance of the signal source. (5%)

2. Figure 2 shows a signal source connected to the input of an amplifier. Here R_s is the source resistance, and R_i and C_i are the input resistance and input capacitance, respectively, of the amplifier. **(15%)**
(a) Find the transfer function $V_i(s)/V_s(s)$. (5%)
(b) Is this a high-pass or low-pass network? (2%)
(c) Sketch Bode magnitude and phase plot of the transfer function as $R_s = 20$kΩ, $R_i = 80$kΩ, and $C_i = 5$ pF. (6%)
(d) What is the 3-dB frequency in (c)? (2%)

3. Based on standard semiconductor fabrication technology, write down the brief run sheet and draw the cross sections of each step to fabricate a typical n-well CMOS as shown in Fig. 3. **(10%)**

4. Figures 4(a) and 4(b) are the physical structure of the enhancement-type MOSFET. **(15%)**
(a) Derive the i_D-v_{DS} characteristics for a NMOS transistor in the triode region and saturation region. (10%)

$$i_D = k_n'\frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \quad \text{(Triode region)}$$

$$i_D = \frac{1}{2}k_n'\frac{W}{L}(v_{GS} - V_t)^2 \quad \text{(Saturation region)}$$

(b) Show the gate-to channel capacitance is approximately $\frac{2}{3}WLC_{OX}$ as the MOSFET operates in saturation, where $C_{OX} = \varepsilon_{ox}/t_{ox}$ is the gate (or oxide) capacitance per unit gate area. (5%)

5. Figure 5 is a particular cascoded current mirror, and all transistors have $V_t = 0.6$ V, $\mu_n C_{ox} = 200$ μA/V^2, $L = 1$ μm, and $V_A = 20$ V. Width $W_1 = W_4 = 2$ μm, and $W_2 = W_3 = 40$ μm. The reference current I_{REF} is 25 μA. **(15%)**
(a) What is the output current? (3%)
(b) What are the voltages at the gates of Q_2 and Q_3? (3%)
(c) What is the lowest voltage at the output for which current-source operation is possible? (3%)
(d) What are the values of g_m and r_o of Q_2 and Q_3? (3%)
(e) What is the output resistance of the mirror? (3%)

6. Figure 6 shows an active-loaded bipolar differential amplifier employing a folded cascode stage (Q_3 and Q_4) and a Wilson current mirror load (Q_5, Q_6, and Q_7). Find G_m and R_{o4}, R_{o5}, R_o and A_d for the differential amplifier in below figure under the following conditions: $I = 1$ mA, $\beta_P = 50$, $\beta_N = 100$, and $V_A = 100$ V. **(15%)**

7. Give two different realizations of the exclusive-OR function $Y = \overline{A}B + A\overline{B}$ in which the pull-down network (PDN) and the pull-up network (PUN) are dual networks. **(15%)**

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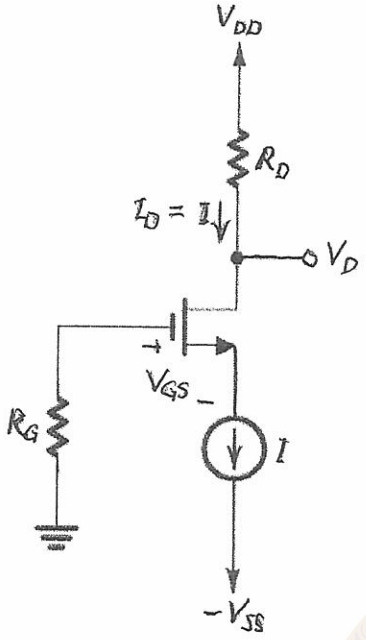

Fig. 1

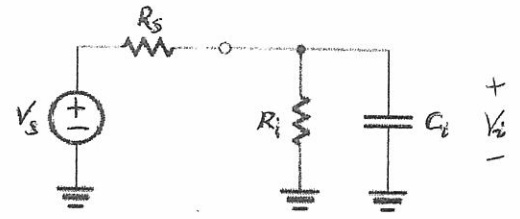

Fig. 2

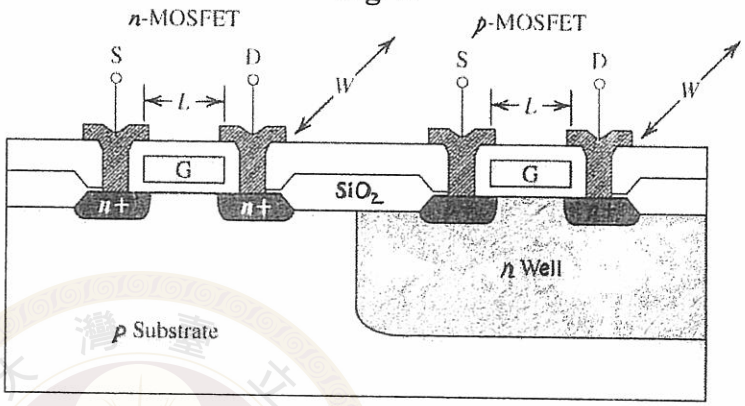

Fig. 3

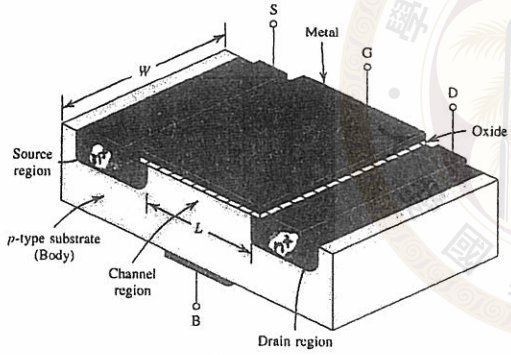

Fig. 4(a)

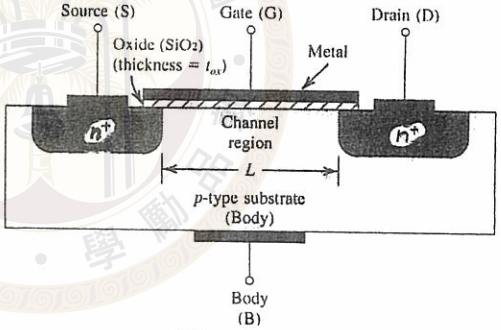

Fig. 4(b)

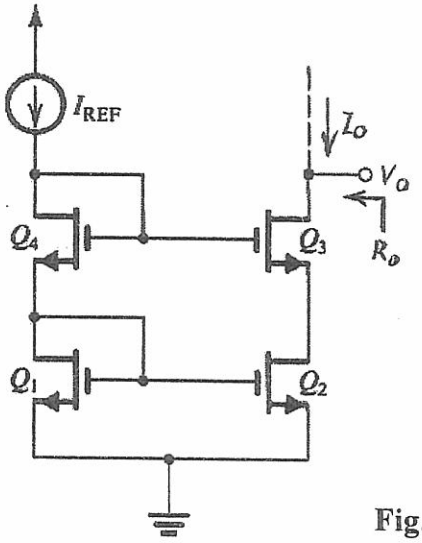

Fig. 5

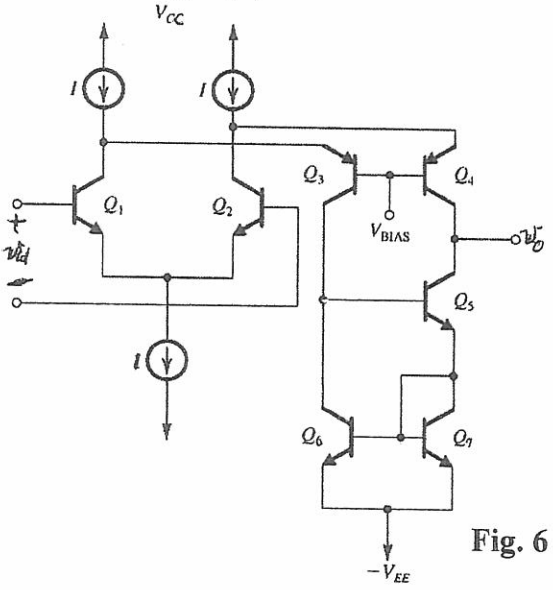

Fig. 6

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