※注意：Part I 題目請於試卷內之「選擇題作答區」依序作答，Part II 請作答於試卷內之「非選擇題作答區」。

Part I (40%): Reading Comprehension (閱讀並回答下列問題於試卷內之「選擇題作答區」):

Article 1: "Semiconductor giants race to make next generation of cutting-edge chips," *Financial Times*, December 11, 2023

The world's leading semiconductor companies are racing to make so-called "2 nanometre" processor chips that will power the next generation of smartphones, data centres and artificial intelligence. Taiwan Semiconductor Manufacturing Company remains the analysts' favourite to maintain its global supremacy in the sector, but Samsung Electronics and Intel have identified the industry's next leap forward as a chance to close the gap.

For decades, chipmakers have sought to make ever more compact products. The smaller the transistors on a chip, the lower the energy consumption and the higher their speed. Today, terms such as "2 nanometre" and "3 nanometre" are widely used as shorthand for each new generation of chip, rather than a semiconductor's actual physical dimensions. Any company that opens up a technological lead in the next generation of advanced semiconductors will be well placed to dominate an industry that pulled in well over $500bn in global chip sales last year. That is projected to grow further due to a surge in demand for the data centre chips that power generative AI services.

TSMC, which dominates the global market in processors, has already shown the process test results for its "N2" — or 2 nanometre — prototypes to some of its biggest customers, including Apple and Nvidia, according to two people with direct knowledge of the discussions. But two people close to Samsung said the Korean chipmaker was offering cut-price versions of its latest 2 nanometre prototypes in an effort to attract the interest of big-name customers including Nvidia. "Samsung sees 2 nanometre as a game-changer," said James Lim, analyst at US hedge fund Dalton Investments. "But people are still doubtful it can execute the migration better than TSMC." Former market leader Intel has also made bold claims about producing its next generation of chips by the end of next year. That could put it back ahead of its Asian rivals, though doubts remain about the performance of the US company's products.

TSMC, which has said that mass production of N2 chips will begin in 2025, typically launches the mobile version first, with Apple as its lead customer. Versions for PC and then high-performance computing chips designed for higher power loads will come later. Apple's latest flagship smartphones, the iPhone 15 Pro and Pro Max, were the first mass-market consumer devices to deploy TSMC's new 3 nanometre chip technology when they were introduced in September this year.

The challenges of moving from one generation, or "node", of process technology to the next intensify as chips keep getting smaller, raising the possibility of a mis-step that could see TSMC's crown slip. TSMC told the Financial Times its N2 technology development was "progressing well and on track for volume production in 2025, and will be the most advanced semiconductor technology in the industry in both density and energy efficiency when it is introduced". But Lucy Chen, vice-president of Isaiah Research, noted the cost of moving to the next node was going up, while improvements in performance had plateaued. "[Moving to the next generation] is not as attractive to customers anymore," said Chen.

Experts stress that mass production is still two years away, and that teething problems are a natural part of the chip production process. Insiders at Samsung, which according to consultancy TrendForce has a 25 percent share of the global advanced foundry market compared with TSMC's 66 percent, see an opportunity to close the gap. The Korean conglomerate was the first to start mass production of its 3nm, or "SF3" chips last year, and the first to make the switch to a new transistor architecture known as "Gate-All-Around" (GAA).

According to two people familiar with the situation, US chip designer Qualcomm is planning to use Samsung's "SF2" chip in its next-generation high-end smartphone processors. That would mark a reversal in fortune after Qualcomm transferred most of its flagship mobile chips from Samsung's 4 nanometre process to TSMC's equivalent. "We are well-equipped to set up

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for SF2 mass production by 2025," Samsung said. "Since we were the first to take the leap and transition to GAA architecture, we are hoping the progress from SF3 to SF2 will be relatively seamless."

Analysts caution that while Samsung was the first to bring its 3nm chips to market, it has struggled with its "yield rate" — the proportion of chips produced that are deemed shippable to customers. The Korean company insists that its 3 nanometre yield rates have improved. But according to two people close to Samsung, the yield rate of its simplest 3nm chip is just 60 percent, well below customer expectations and likely to fall further when producing more complex chips equivalent to Apple's A17 Pro or Nvidia's graphic processing units.

"Samsung tries to do these quantum leaps," said Dylan Patel, chief analyst at research firm SemiAnalysis. "They can claim all they want, but they still have not released a proper 3 nanometre chip." Lee Jong-hwan, professor of system semiconductor engineering at Sangmyung University in Seoul, added that Samsung also suffered from the fact that its smartphone and chip design divisions were fierce competitors of the potential customers for the logic chips produced in its foundry division. "Samsung's structure causes concern to many potential customers about possible tech or design leaks," said Lee.

Meanwhile, former market leader Intel is promoting its next generation "18A" node at technology conferences and offering free test production to chip design firms. The US company says it is set to begin production of 18A in late 2024, potentially making it the first chipmaker to migrate to the next generation. But CC Wei, TSMC's chief executive, appears unfazed. He said in October that according to the Taiwanese company's internal assessment its latest 3 nanometre variant, which is already on the market, is comparable to Intel's 18A in terms of power, performance and density.

Both Samsung and Intel also hope to benefit from potential customers looking to reduce their dependence on TSMC, whether for commercial reasons or out of concern about a potential Chinese threat to Taiwan. In July, the chief executive of US chipmaker AMD said it would "consider other manufacturing capabilities" besides those offered by TSMC, as it pursued greater "flexibility". Leslie Wu, chief executive of consulting firm RHCC, said major customers who require technology at the 2 nanometre level are looking to spread their chip production across multiple foundries. "It's too risky to rely on TSMC solely." But Mark Li, Asia semiconductor analyst at Bernstein, questioned "how meaningful that [geopolitical] factor is compared to factors such as efficiency and schedule is open to debate. TSMC remains superior when it comes to cost, efficiency and trust."

Answer the following questions. For Questions 1-4, select <u>one</u> answer choice:

1. (5%) According to Article 1, what is the current state-of-art technological generation of chips in the semiconductor industry?
   a. 2 nanometre
   b. 3 nanometre
   c. 4 nanometre
2. (5%) According to Article 1, which company is anticipated to transition to the next technological generation first?
   a. Intel
   b. TSMC
   c. Samsung
3. (5%) According to Article 1, why does moving to the next technological generation become harder?
   a. Declining costs of upgrading attract more potential competitors
   b. Marginal improvements in performance are diminishing
   c. The yield rate has decreased considerably
4. (5%) According to Article 1, what is the transistor architecture that Samsung is currently using?
   a. SF2
   b. SF3
   c. Gate-All-Around

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For the following questions, consider each of the choices separately and select all that apply:

5. (10%) According to Article 1, which of the following statement(s) is/are true?
   a. In the year 2021, Qualcomm engaged with a contract with TSMC.
   b. TSMC tends to launch the mobile and PC versions of new chips simultaenously.
   c. Terms "2 nanometre" and "3 nanometre" reflect the actual size of chips.
   d. TSMC's current 3 nanometre chips are equivalent to Intel's new 2 nanometre chips in terms of performance.
   e. The market share of TSMC is twice that of Samsung.
6. (10%) Which of the following statements are mentioned in Article 1 on Samsung's leapfrogging strategy?
   a. A geopolitical factor will trivially complement Samsung to catch up TSMC in 2 nanometre generation.
   b. Samsung's organizational structure will safeguard the confidentiality of its technology and design.
   c. To attract the interest of customers, Samsung will offer the cut-price version of 3 nanometre chips.
   d. Samsung believes that the transition from 3 nanometers to 2 nanometers will be smooth, given its status as the first adopter of the Gate-All-Around architecture.
   e. Samsung's low yield rates have remained below the expectations of customers.

Part II (60%): Analytical Writing (分析寫作；作答於試卷內之「非選擇題作答區」)

Read the following articles, and then plan and compose a response to the issue below. Responding to any other issue will receive a score of zero. Be sure to respond according to the specific instructions and support your position on the issue with reasons and examples drawn from such areas as your reading, experience, observations, and/or academic studies.

Article 2: Excerpts of "Comparing FinFETs vs. GAAFETs," Cadence System Analysis, December 30, 2022.

During the mid-20th century, complementary metal-oxide semiconductors (CMOS) were a remarkable invention for the electronics industry. CMOS technology started the trend of miniaturization and performance enhancement in semiconductor electronics, especially in integrated circuit applications. CMOS technology introduced planar transistors with low costs, low power consumption, and high packing density. The downsizing of planar transistors continued with advanced manufacturing processes. However, the scaling of CMOS planar transistors brought numerous problems such as gate leakage currents, short channel effects, quantum tunneling leakage, variability, mobility degradation, etc.

The development of multigate devices such as finFETs and GAAFETs are innovations in transistor technology that offset planar transistors. FinFET technology emerged as a solution for planar transistor-induced problems by opening the scope for three-dimensional (3D) transistor construction. GAAFETs confirm 3D technology in semiconductor transistor fabrication and help overcome the limitations of finFET. In this article, we will compare finFET vs. GAAFET technologies ...(omitted)...

FinFETs and GAAFETs utilize a non-planar transistor structure that increases the speed and performance of devices with reduced power consumption and footprint. ...(omitted)... By comparing finFET vs. GAAFET technologies, it can be summarized that gate-all-around transistors are the future of integrated circuits. Their design flexibility, low operational voltage, high drive currents, high computational speed, and excellent performance within a smaller footprint area will continue to make them advantageous. ...(omitted)

Article 3: Excerpts of "Highlights of the day: TSMC reportedly adopts GAA transistors for 2nm chips," DIGITIMES Asia, September 21, 2020.

TSMC's has disclosed that its 3nm process will continue to adopt a FinFET structure, but the foundry reportedly will take a new approach to its 2nm chip development, replacing FinFET with GAA transistors. Meanwhile, strong demand for high-performance CPU, GPU, AI and networking chips has booked up production capacity at Taiwanese ABF substrate makers throughout first-half 2021. Surging demand for Chromebooks in support of remote learning has created shortages SOEM key components, and revived orders for HDDs.

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According to Articles 1, 2, and 3, TSMC, the market champion, lagged behind in transitioning from an old transistor architecture to a new one. Two competing explanations can be proposed to understand why a market champion like TSMC tends to be inertial in adopting a new technological standard.

Argument 1 (Irrational market leader) - The managers of leading companies might prioritize maximizing short-term profits from current products instead of making forward-looking investments in new ones. Additionally, the upper management of these companies dismissed new products as unimportant, allocating more budgets and engineers to the established product group over the new one. Lastly, the customers of existing products played a significant role in the current profits of these companies, leading top management to prioritize the ongoing business.

Argument 2 (Rational market leader concerns replacement effects) - The benefits of introducing a new product may be smaller for market-leading companies than for followers, depending on the extent to which the old and new goods substitute for each other. Consequently, leading companies may perceive the introduction of new products as merely replacing their old source of profits.

The above arguments draw from the following source: *Estimating the Innovator's Dilemma: Structural Analysis of Creative Destruction in the Hard Disk Drive Indus*try, 1981-1998, The Journal of Political Economy, May, 2017, Vol. 125, No. 3, Mitsuru Igami.

Write a response in which you discuss your perspective on which explanation is more relevant to the observed delay of TSMC compared to Samsung and Intel.

You should write no less than 300 words, but no more than 1000 words. Your response will be evaluated for its overall quality based on how well you:

- Respond to the specific task instructions
- Consider the complexities of the issue
- Organize, develop, and express your ideas
- Support your ideas with relevant reasons and/or examples
- Control the elements of standard written English

Before beginning writing, you may want to think for a few minutes and then plan your response. **Use the bottom of this page to plan your response, and then write your response in the answer sheets (試卷內之「非選擇題作答區」).** Be sure to develop your positions completely and organize it coherently, but spare some time to proof-read what you have written to make any revisions you deem necessary.

Plan Your Response Here -- Write Your Essay in the Answer Sheets (試卷內之「非選擇題作答區」)

This page will not be scored.

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