1. (70%) For the following circuit, please

(a) (10%) identify the non-inverting input node ($V_1$ or $V_2$),

(b) (10%) find $V_{BN1}$ and $V_{BP1}$ such that $I_{DS3}$=200uA and $I_{DS4}$=$I_{DS5}$=250uA,

(c) (10%) find the static power consumption,

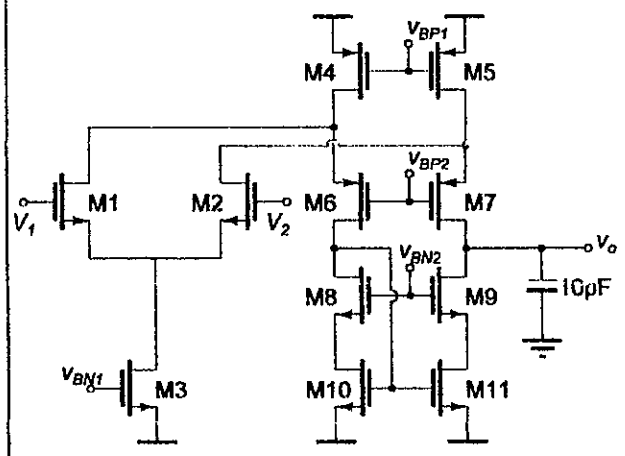
(d) (10%) find the input common mode range of the amplifier (ICMR+ and ICMR-),

(e) (10%) find $V_{BP2}$ and $V_{BN2}$ such that the output voltage range can be maximized,

(f) (10%) find the differential-mode gain ( $A_{vd}$=$|v_o/(v_1-v_2)|$ ), and

(g) (10%) plot the Bode plot (both gain and phase).

[$V_{DD}$=+5V, $V_{SS}$=-5V, $\mu_n C_{ox}$=100μA/V², $\mu_p C_{ox}$=50μA/V², $V_{tn}$= -$V_{tp}$ =0.5V, and λ=0.05. Please assume all transistors are biased correctly in the saturation region and all have ratios of 16/1.]




2. (30%) An amplifier has a low-frequency gain of 80 dB and three poles at 1 kHz, 1 MHz, and 100 MHz, respectively.

(a) (10%) Please plot the Bode plot of the amplifier (both gain and phase),

(b) (10%) find the phase margin of the open-loop amplifier, and

(c) (10%) find β such that the amplifier has a phase margin of 45 degrees when configured as a closed-loop amplifier.

試題隨卷繳回